SGMOP07
3MHz, Low Noise, High Voltage, Precision Operational Amplifier

GENERAL DESCRIPTION

The SGMOP07 is a low noise, low offset voltage and high voltage operational amplifier, which can be designed into a wide range of applications. The SGMOP07 has a high gain-bandwidth product of 3MHz, a slew rate of 4V/μs, and a quiescent current of 0.9mA at wide power supply range.

The SGMOP07 is designed to provide optimal performance in low noise systems. It provides rail-to-rail output swing into heavy loads.

The single SGMOP07 is available in Green SOIC-8 package. It is specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Rail-to-Rail Output**
- **Low Bias Current: ±1nA (TYP)**
- **High Open-Loop Gain: 120dB at V_S = ±15V**
- **High PSRR: 146dB**
- **High Gain-Bandwidth Product: 3MHz**
- **Settling Time to 0.1% with 1V Step: 0.5μs**
- **Overload Recovery Time: 10μs**
- **Low Noise: 8.5nV/$\sqrt{Hz}$ at 1kHz**
- **Supply Voltage Range:**
  3.6V to 36V or ±1.8V to ±18V
- **Input Common Mode Voltage Range:**
  ($-V_S$) + 1.5V to ($+V_S$) - 2V
- **Low Quiescent Current: 0.9mA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8 Package**

APPLICATIONS

Sensors
Audio
Active Filters
A/D Converters
Communications
Test Equipment
Cellular and Cordless Phones
Laptops and PDAs
Photodiode Amplification

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGMOP07	SOIC-8	-40℃ to +125℃	SGMOP07XS8G/TR	SGM OP07XS8 XXXXX	Tape and Reel, 2500

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Common Mode Voltage Range
.... $(-V_S) - 0.3V$ to $(+V_S) + 0.3V$
Storage Temperature Range .... -65℃ to +150℃
Junction Temperature .... +150℃
Lead Temperature (Soldering 10sec) .... +260℃
ESD Susceptibility
HBM 2000V
MM 200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .... 3.6V to 36V
Operating Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

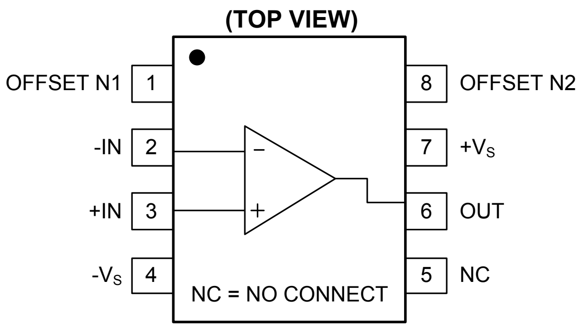
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



SOIC-8

ELECTRICAL CHARACTERISTICS

(At T_A = +25℃, V_S = ±5V to V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V and R_L connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage	V_{OS}		+25℃		100	170	μV
			Full			290	
Input Bias Current	I_B	$V_{CM} = V_S/2$	+25℃		±1	±16	nA
			Full			±55	
Input Offset Current	I_{OS}	$V_{CM} = V_S/2$	+25℃		±1	±18	nA
			Full			±28	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ + 1.5		$(+V_S)$ - 2	V
Common Mode Rejection Ratio	CMRR	$(-V_S) + 1.5V \le V_{CM} \le (+V_S) - 2V$	+25℃	115	140		dB
			Full	113			
Open-Loop Voltage Gain	A_{OL}	V_S = ±5V, V_{OUT} = ±2.5V, R_L = 10kΩ	+25℃	112	135		dB
			Full	110			
		V_S = ±15V, V_{OUT} = ±10V, R_L = 10kΩ	+25℃	115	126		
			Full	109			
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 2kΩ	+25℃	105	112		
			Full	94			
		V_S = ±15V, V_{OUT} = ±10V, R_L = 2kΩ	+25℃	112	120		
			Full	102			
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		0.5		μV/℃
OFFSET ADJUSTMENT							
Offset Adjustment Range		R_S = 50kΩ, See Figure 1	+25℃		±20		mV
External Resistance between OFFSET N1 and $+V_S$			+25℃	15			kΩ
External Resistance between OFFSET N2 and $+V_S$			+25℃	15			kΩ
OUTPUT CHARACTERISTICS							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±15V, R_L = 10kΩ	+25℃		90	175	mV
			Full			220	
		V_S = ±15V, R_L = 2kΩ	+25℃		450	850	
			Full			1060	
Output Short-Circuit Current	I_{SC}		+25℃	±13	±32		mA
POWER SUPPLY							
Operating Voltage Range	V_S		Full	3.6		36	V
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0mA	+25℃		0.9	1.2	mA
			Full			1.3	
Power Supply Rejection Ratio	PSRR	V_S = 3V to 38V	+25℃	121	146		dB
			Full	118			

ELECTRICAL CHARACTERISTICS (continued)

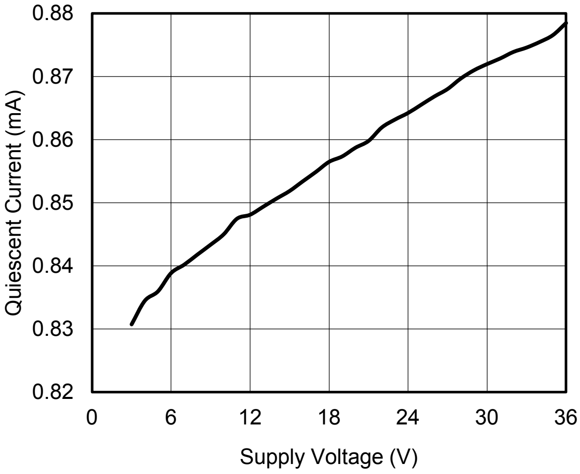
(At T_A = +25℃, V_S = ±5V to V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V and R_L connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Gain-Bandwidth Product	GBP	V_{OUT} = 100mV_{P-P}, R_L = 2kΩ, C_L = 10pF	+25℃		3		MHz
Slew Rate	SR	R_L = 2kΩ	+25℃		4		V/μs
Settling Time to 0.1%	t_S	V_{IN} = 1V Step, R_L = 2kΩ, G = +1	+25℃		0.5		μs
Overload Recovery Time		R_L = 2kΩ, V_{IN} × G = V_S	+25℃		10		μs
Phase Margin	$φ_O$	V_{OUT} = 100mV_{P-P}, R_L = 2kΩ, C_L = 10pF	+25℃		55		°
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 1V_{RMS}, G = +1, R_L = 2kΩ, f = 1kHz	+25℃		0.0008		%
NOISE							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		300		nV_{P-P}
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		8.5		nV/$\sqrt{Hz}$
Input Current Noise Density	i_n	f = 1kHz	+25℃		1.5		pA/$\sqrt{Hz}$

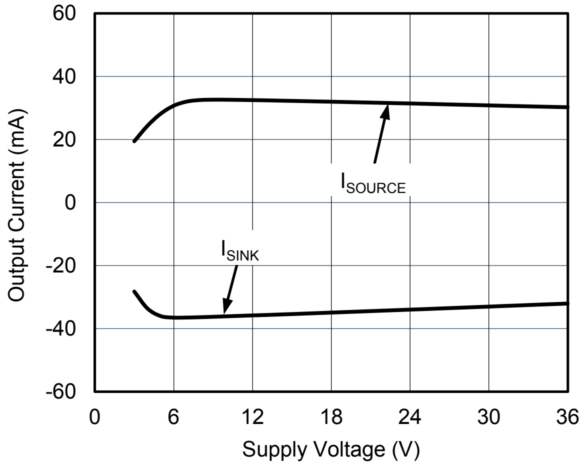
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃ and V_S = ±15V, unless otherwise noted.

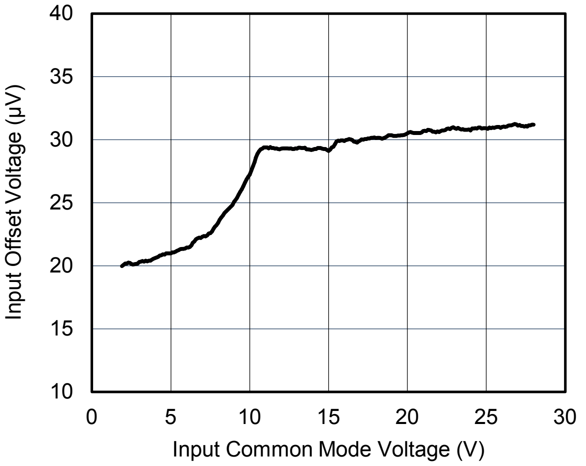
Quiescent Current vs. Supply Voltage



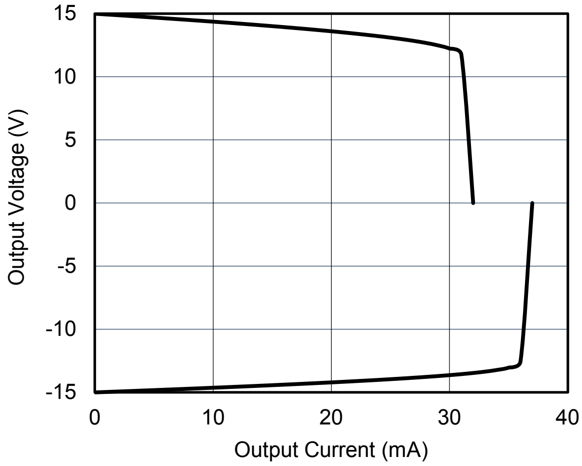
Output Current vs. Supply Voltage



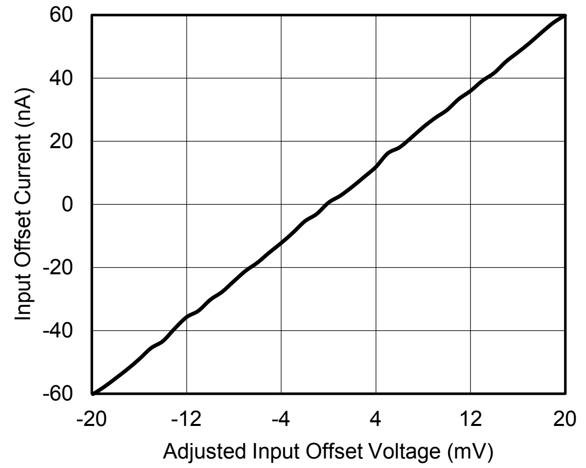
Input Offset Voltage vs. Input Common Mode Voltage



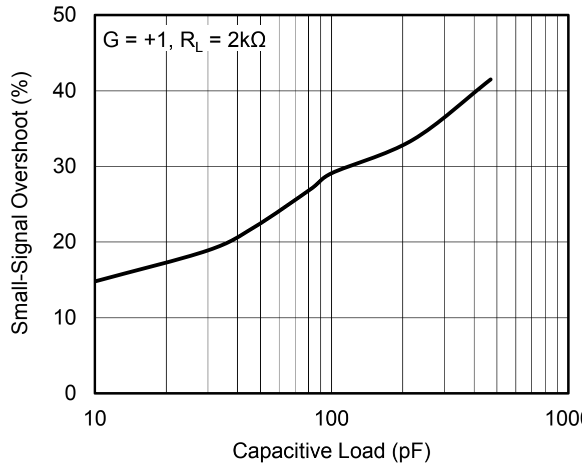
Output Voltage vs. Output Current



Input Offset Current vs. Adjusted Input Offset Voltage



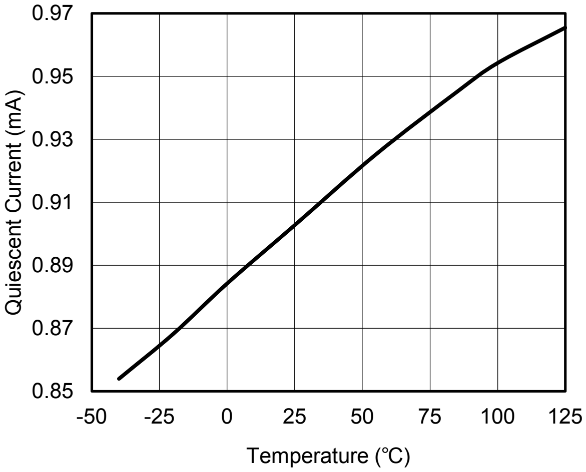
Small-Signal Overshoot vs. Capacitive Load



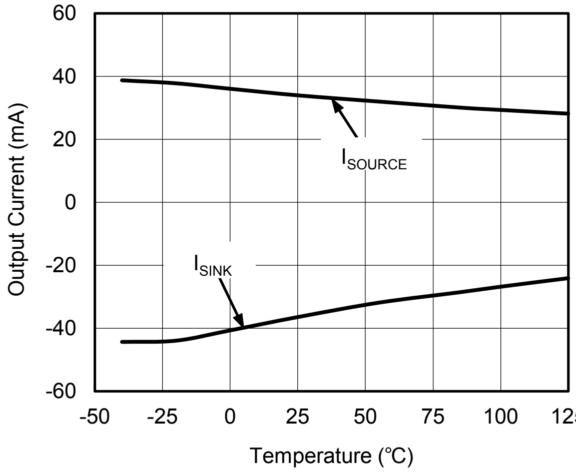
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃ and V_S = ±15V, unless otherwise noted.

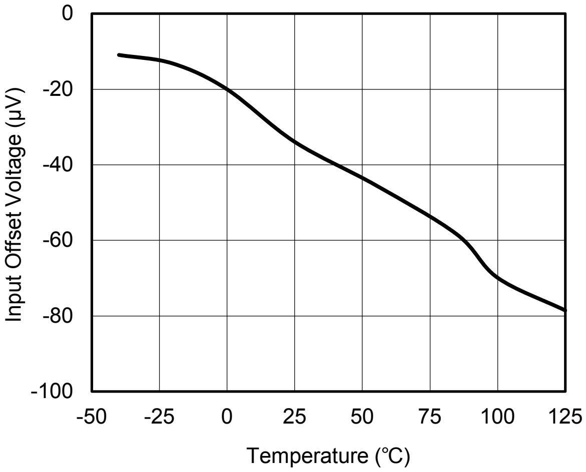
Quiescent Current vs. Temperature



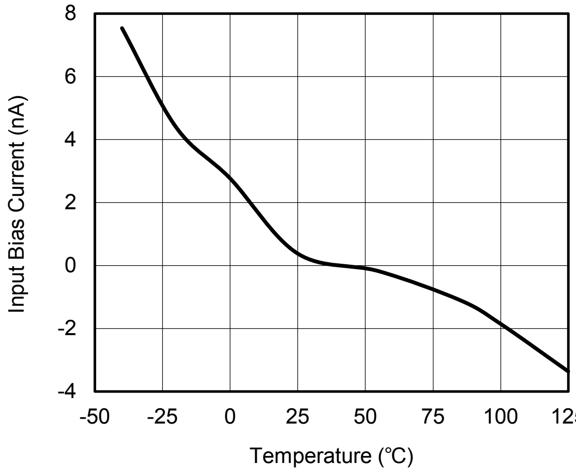
Output Current vs. Temperature



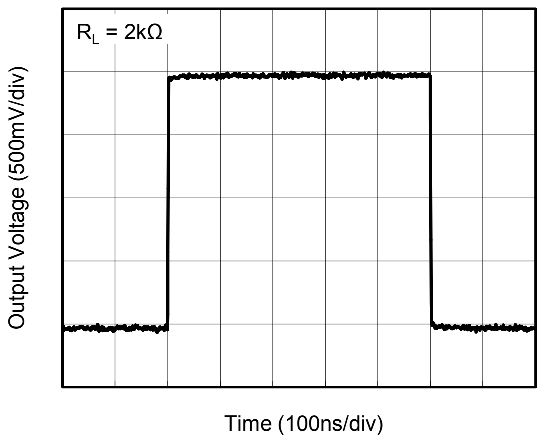
Input Offset Voltage vs. Temperature



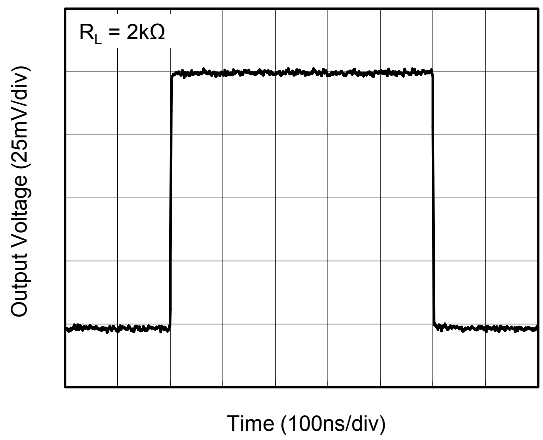
Input Bias Current vs. Temperature



Large-Signal Step Response

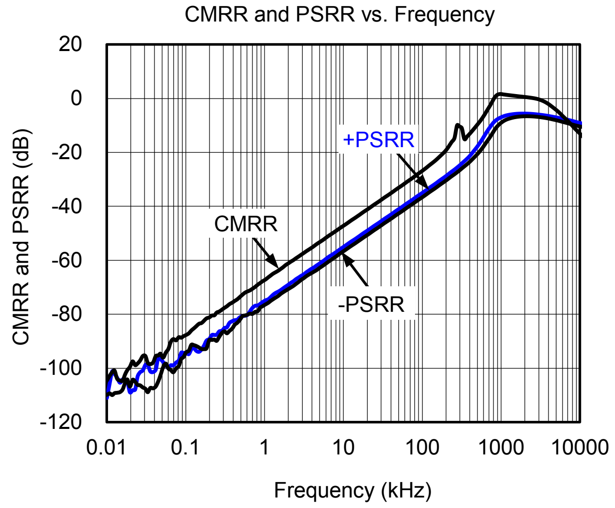


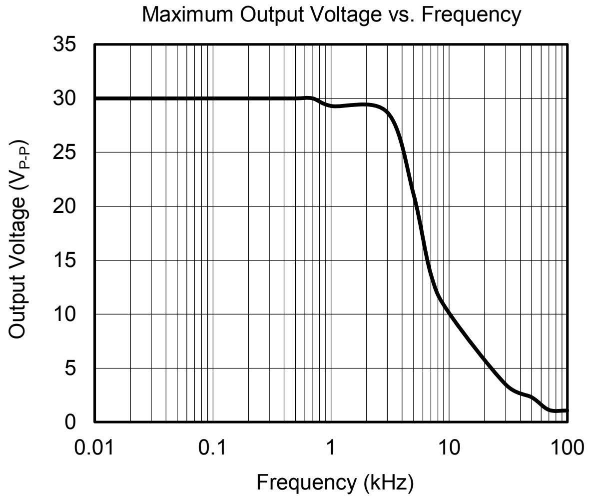
Small-Signal Step Response

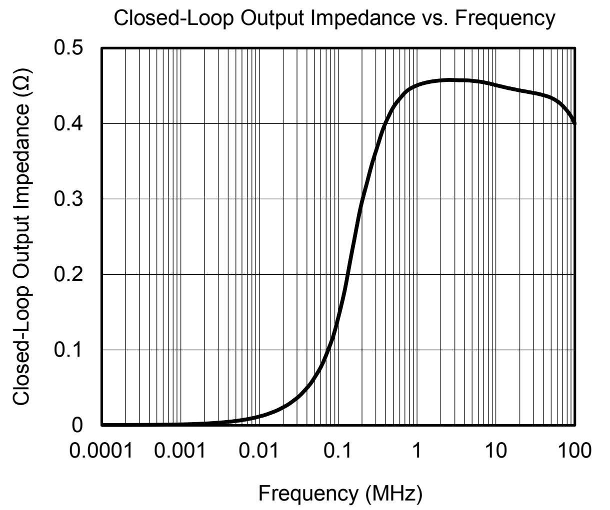


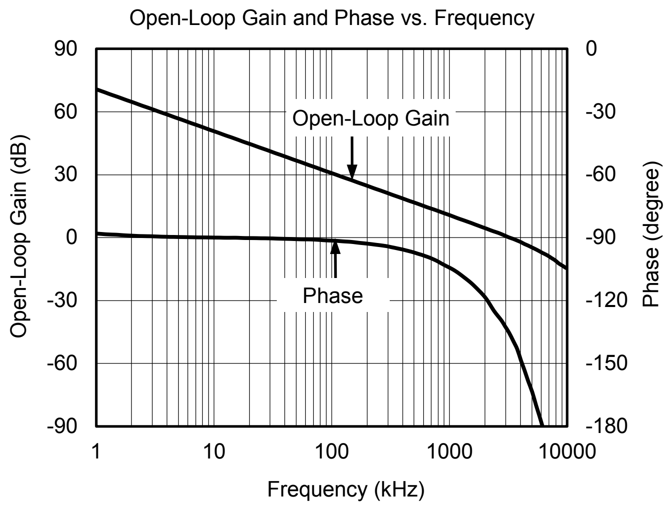
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

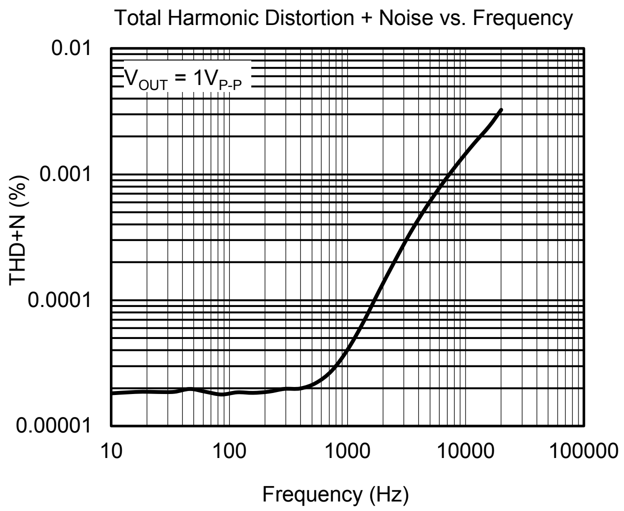
At T_A = +25℃ and V_S = ±15V, unless otherwise noted.

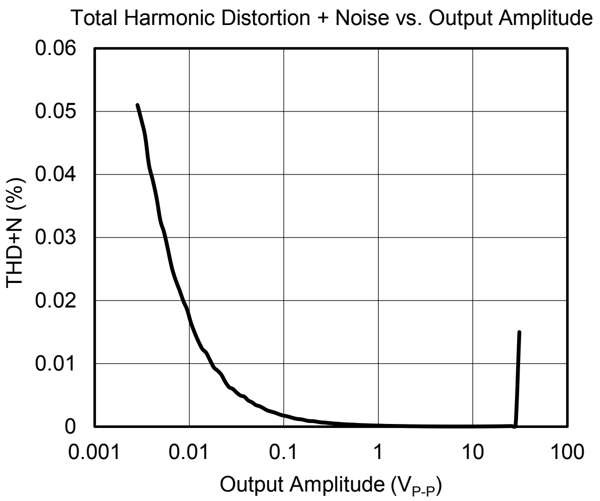








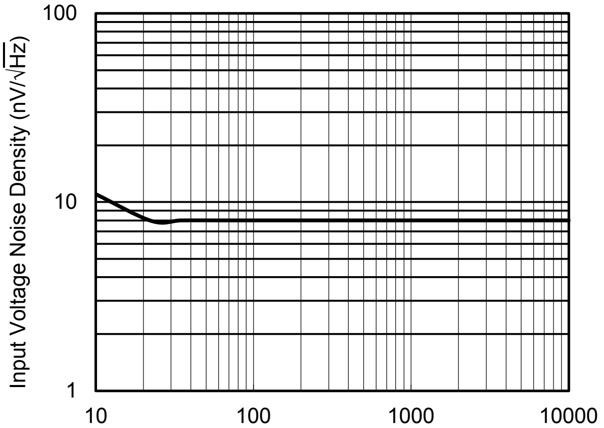




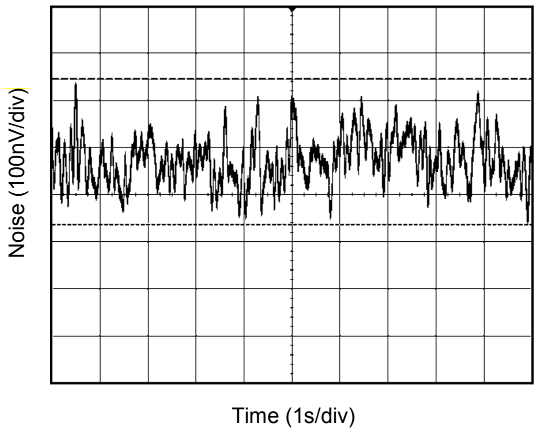
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃ and V_S = ±15V, unless otherwise noted.

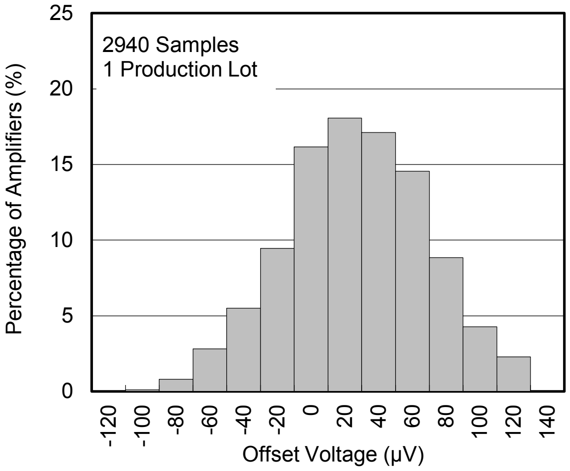
Input Voltage Noise Density vs. Frequency



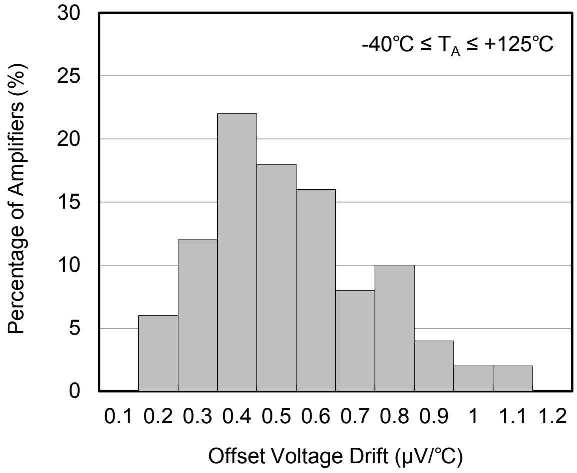
0.1Hz to 10Hz Input Voltage Noise



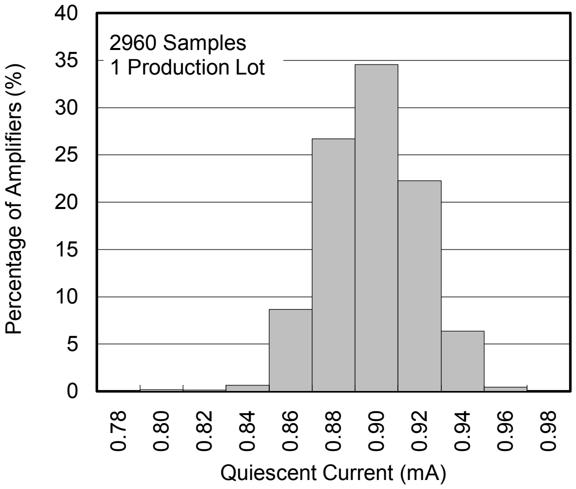
Offset Voltage Production Distribution



Offset Voltage Drift Distribution



Quiescent Current Production Distribution



APPLICATION NOTES

General Application

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain-betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in Figure 1. A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. The resistance between OFFSET N1 and $+V_S$ should not be less than 15kΩ. Similarly, the resistance between OFFSET N2 and $+V_S$ should not be less than 15kΩ.

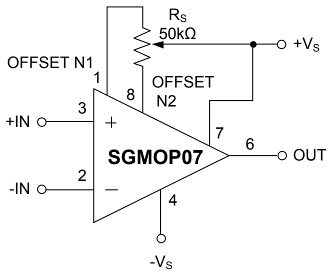


Figure 1. Input Offset-Voltage Null Circuit

Power-Supply Bypassing and Layout

The SGMOP07 operates from either a single 3.6V to 36V supply or dual ±1.8V to ±18V supplies. For single-supply operation, bypass the power supply $+V_S$ with a 0.1μF ceramic capacitor which should be placed close to the $+V_S$ pin. For dual-supply operation, both the $+V_S$ and the $-V_S$ supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. A 10μF tantalum capacitor can be added for better performance.

Good PCB layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency current loop area small to minimize the EMI (electromagnetic interference).

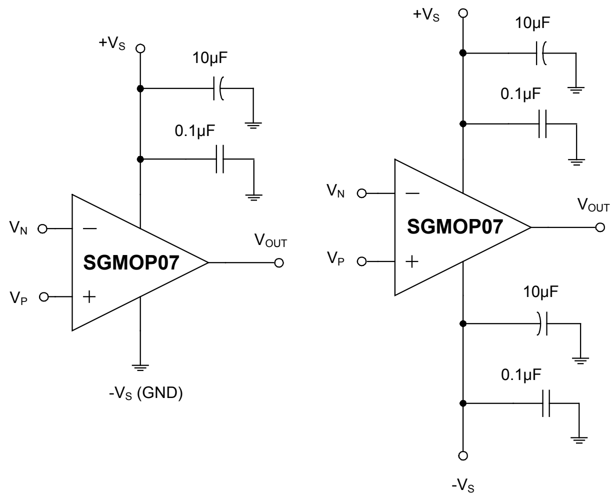


Figure 2. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for SGMOP07 circuit design. The length of the current path in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be in parallel. This helps reduce unwanted positive feedback.

Differential Amplifier

The circuit shown in Figure 3 performs the difference function. If the resistor ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

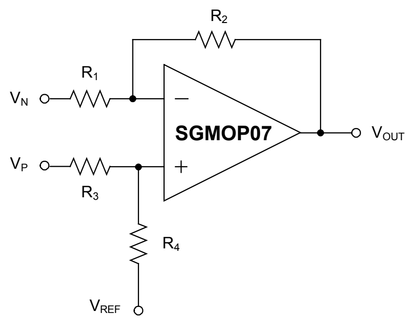


Figure 3. Differential Amplifier

APPLICATION NOTES (continued)

Instrumentation Amplifier

The circuit in Figure 4 performs the same function as that in Figure 3 but with a high input impedance.

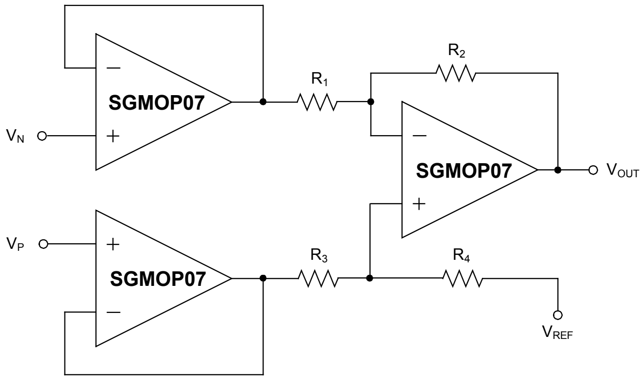


Figure 4. Instrumentation Amplifier

Active Low-Pass Filter

The low-pass filter shown in Figure 5 has a DC gain of $(-R_2/R_1)$ and the -3dB corner frequency is $1/2\pi R_2C$. Make sure the filter bandwidth is within the bandwidth of the amplifier. Feedback resistors with large values can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistor values as low as possible and consistent with output loading consideration.

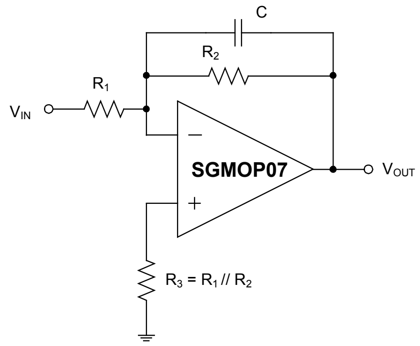


Figure 5. Active Low-Pass Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2017 – REV.A to REV.A.1

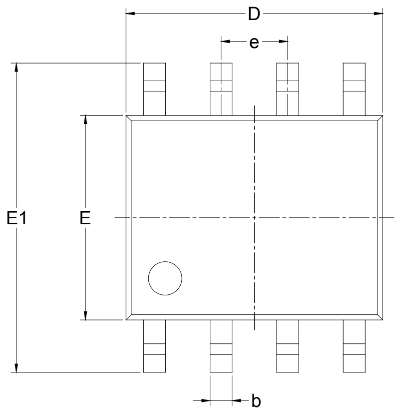
Added external resistance parameter	3
Updated open-loop gain and phase vs. frequency	7

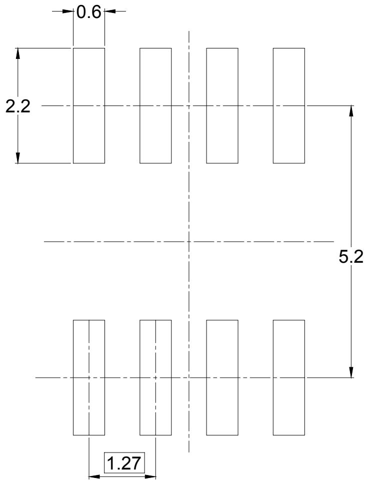
Changes from Original (AUGUST 2017) to REV.A

Changed from product preview to production data	All

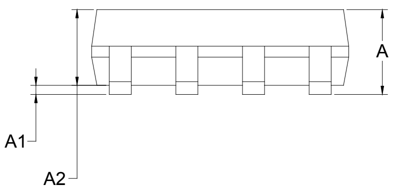
PACKAGE OUTLINE DIMENSIONS

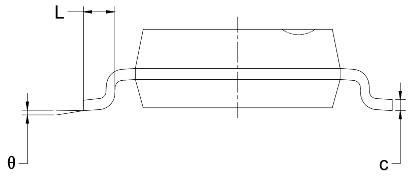
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

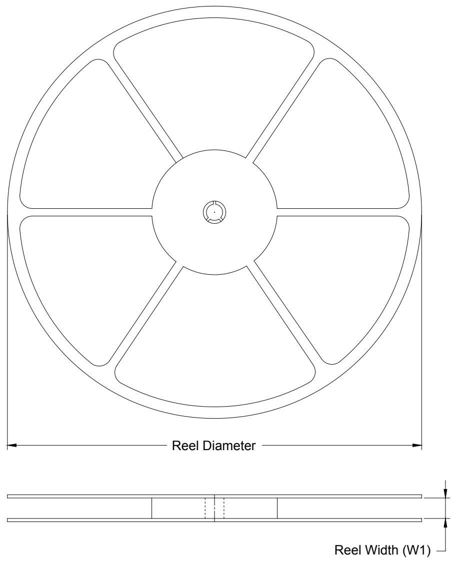




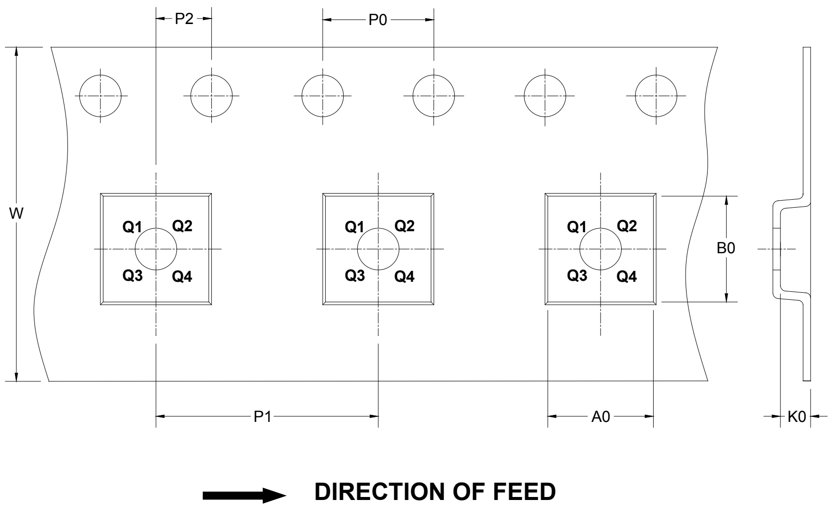
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



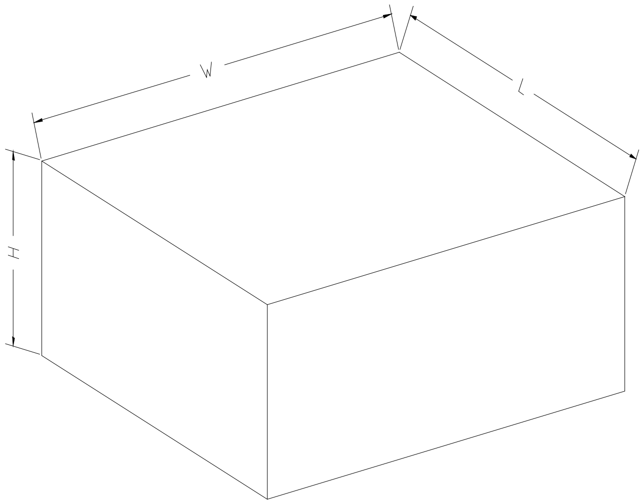
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002