SBVS197C – MAY 2013 – REVISED JULY 2013

2-A, 6-μV_{RMS}, RF, LDO Voltage Regulator

Check for Samples: TPS7A8300

FEATURES

- **Ultralow Dropout: 125 mV Maximum at 2 A**
- **Output Voltage Noise: 6 μV_{RMS}**
- **Power-Supply Ripple Rejection:**
  - **40 dB at 1 MHz**
- **Input Voltage Range:**
  - **Without BIAS: +1.4 V to +6.5 V**
  - **With BIAS: +1.1 V to +6.5 V**
- **Two Output Voltage Modes:**
  - **ANY-OUT™ Version (User-Programmable Output via PCB Layout):**
    - **No External Resistor or Feed-Forward Capacitors Required**
    - **Output Voltage Range: +0.8 V to 3.95 V**
  - **Adjustable Version:**
    - **Output Voltage Range: +0.8 V to 5.0 V**
- **1.0% Accuracy Over Line, Load, and Temperature**
- **Stable with a 22-µF Output Ceramic Capacitor**
- **Programmable Soft-Start and Power-Good (PG) Output**
- **Available Packages:**
  - **5-mm × 5-mm QFN-20**
  - **3,5-mm × 3,5-mm QFN-20 (1)**

(1) 3,5-mm × 3,5-mm QFN-20 package is product-preview.

APPLICATIONS

- **RF, IF Components: VCO, ADC, DAC, LVDS**
- **Wireless Infrastructure: SerDes, FPGA, DSP™**
- **Test and Measurement**
- **Instrumentation, Medical, and Audio**

DESCRIPTION

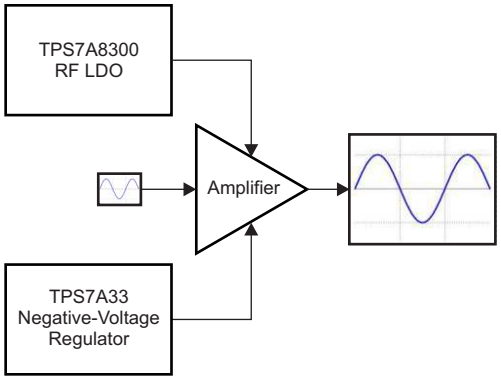
The TPS7A8300 is a low-noise (6 μV_{RMS}), low-dropout voltage regulator (LDO) capable of sourcing a 2-A load with only 125 mV of maximum dropout.

The TPS7A8300 output voltages are fully user-adjustable (up to 3.95 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count. For higher output voltage applications, the device achieves output voltages up to 5 V with the use of external resistors. The device supports very low input voltages (down to 1.1 V) with the use of an additional BIAS rail.

With very high accuracy (1% over line, load, and temperature), remote sensing, and soft-start capabilities to reduce inrush current, the TPS7A8300 is ideal for powering high-current, low-voltage devices such as high-end microprocessors and field-programmable gate arrays (FPGAs).

The TPS7A8300 is designed to power-up noise-sensitive components in high-speed communication applications. The very low-noise, 6-μV_{RMS} device output and high broad-bandwidth PSRR (40 dB at 1 MHz) minimizes phase noise and clock jitter in high-frequency signals. These features maximize performance of clocking devices, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs).

For applications where positive and negative low-noise rails are required, consider TI's TPS7A33 family of negative high-voltage, ultralow-noise linear regulators.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION
TPS7A8300**YYYZ**	**YYY** is the package designator. **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage	IN, BIAS, PG, EN	–0.3	+7.0	V
	IN, BIAS, PG, EN (5% duty cycle)	–0.3	+7.5	V
	SNS, OUT	–0.3	V_{IN} + 0.3(2)	V
	NR/SS, FB	–0.3	+3.6	V
	50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	–0.3	V_{OUT} + 0.3	V
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Temperature	Operating junction temperature, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings(3)	Human body model (HBM), JESD22-A114A		2	kV
	Charged device model (CDM), JESD22-C101B.01		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7.0 V, whichever is smaller.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A8300 RGW (QFN) 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	35.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.6	
θ_{JB}	Junction-to-board thermal resistance	15.2	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	15.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}[1], V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V[2], $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND[3], V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.
Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range		1.1		6.5	V
V_{BIAS}	Bias supply voltage range[1]		3.0		6.5	
$V_{(REF)}$	Reference voltage	$V_{(REF)}$ = $V_{(FB)}$ = $V_{(NR/SS)}$		0.8		V
$V_{UVLO1(IN)}$	Input supply UVLO with BIAS	V_{IN} increasing		1.02	1.085	V
$V_{HYS1(IN)}$	$V_{UVLO1(IN)}$ hysteresis			320		mV
$V_{UVLO2(IN)}$	Input supply UVLO without BIAS	V_{IN} increasing		1.31	1.39	V
$V_{HYS2(IN)}$	$V_{UVLO2(IN)}$ hysteresis			253		mV
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} increasing		2.83	2.9	V
$V_{HYS(BIAS)}$	$V_{UVLO(BIAS)}$ hysteresis			290		mV
V_{OUT}	Output voltage range	Using voltage setting pins (50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V)	0.8 – 1.0%		3.95 + 1.0%	V
		Using external resistors	0.8 – 1.0%		5.0 + 1.0%	V
	Output voltage accuracy[4][5]	0.8 V ≤ V_{OUT} ≤ 5 V, 5 mA ≤ I_{OUT} ≤ 2 A	–1.0		+1.0	%
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V, 5 mA ≤ I_{OUT} ≤ 1.2 A	–1.0		+1.0	%
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 5 mA, 1.4 V ≤ V_{IN} ≤ 6.5 V		0.003		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	5 mA ≤ I_{OUT} ≤ 2 A		0.0001		%/A
$V_{(DO)}$	Dropout voltage	V_{IN} ≥ 1.4 V and V_{BIAS} open, 0.8 V ≤ V_{OUT} ≤ 5.0 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 5.0 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			125	mV
$I_{(LIM)}$	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} = $V_{OUT(TARGET)}$ + 300 mV	2.1	3.4	4.2	A
$I_{(GND)}$	GND pin current	Minimum load, V_{IN} = 6.5 V, no V_{BIAS} supply, I_{OUT} = 5 mA		2.8	4	mA
		Maximum load, V_{IN} = 1.4 V, no V_{BIAS} supply, I_{OUT} = 2 A		3.7	5	mA
		Shutdown, PG = (open), V_{IN} = 6.5 V, no V_{BIAS} supply, $V_{(EN)}$ = 0.5 V			2.5	µA
$I_{(EN)}$	EN pin current	V_{IN} = 6.5 V, no V_{BIAS} supply, $V_{(EN)}$ = 0 V and 6.5 V	–0.1		0.1	µA
$I_{(BIAS)}$	BIAS pin current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, $V_{OUT(TARGET)}$ = 0.8 V, I_{OUT} = 2 A		2.3	3.5	mA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.
(2) $V_{OUT(TARGET)}$ is the calculated V_{OUT} target value from the output voltage setting pins: 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, and 1.6 V in a fixed configuration. In an adjustable configuration, $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors.
(3) This 50-Ω load is disconnected when the test conditions specify an I_{OUT} value.
(4) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5 V and I_{OUT} = 2 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

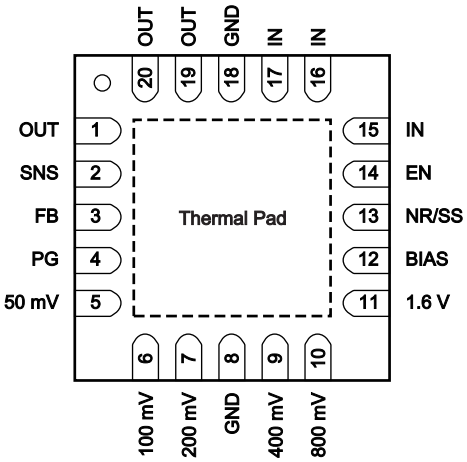
ELECTRICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V(2), $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND(3), V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.
Typical values are at T_J = +25°C.

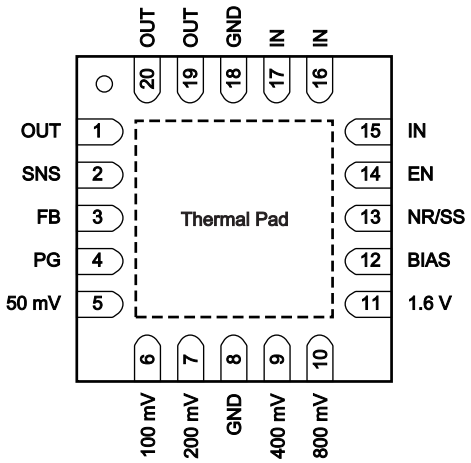
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(PG)}$	PG pin threshold	For the direction PG↓ with decreasing V_{OUT}	0.82 V_{OUT}	0.872 V_{OUT}	0.93 V_{OUT}	V
$V_{hys(PG)}$	PG pin hysteresis	For PG↑		0.02 V_{OUT}		V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, $V_{(PG)}$ = 6.5 V			1	µA
$I_{(NR/SS)}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, V_{IN} = 6.5 V	4.0	6.2	9.0	µA
I_{FB}	FB pin leakage current	V_{IN} = 6.5 V	–100		+100	nA
PSRR	Power-supply ripple rejection	f = 1 MHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		40		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		6		μV_{RMS}
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature		–40		+125	°C

PIN CONFIGURATIONS

RGW PACKAGE
5-mm × 5-mm QFN-20
(TOP VIEW)



RGR PACKAGE(1)
3,5-mm × 3,5-mm QFN-20
(TOP VIEW)

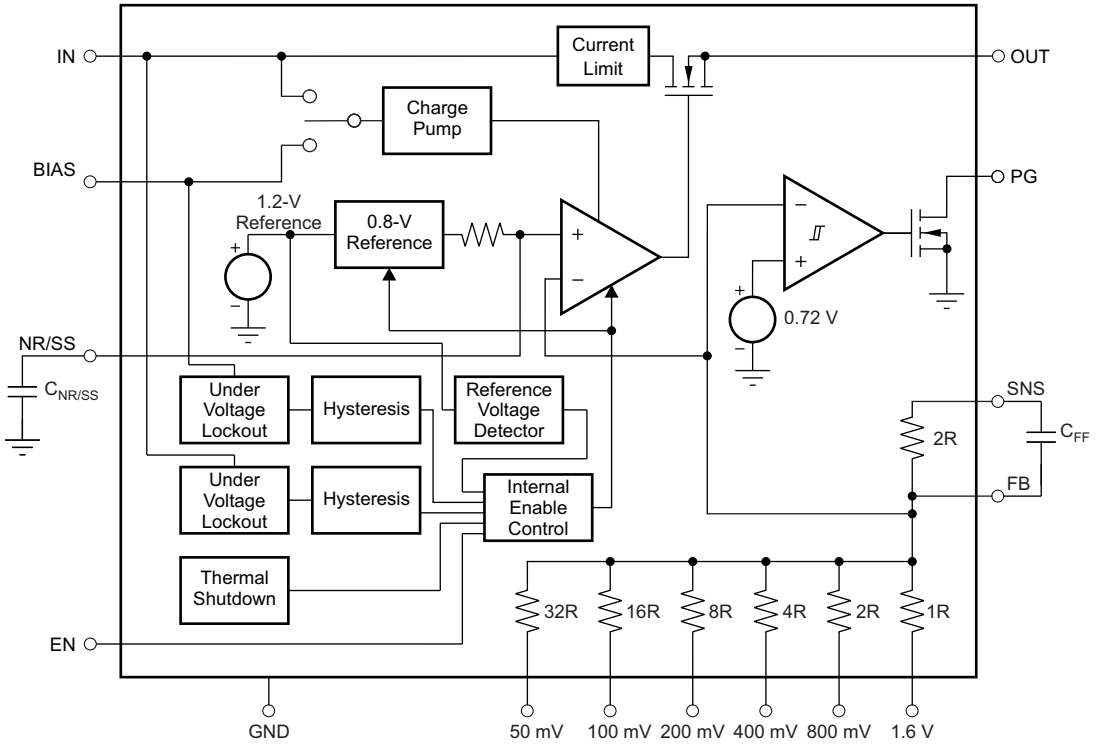


(1) 3,5-mm × 3,5-mm QFN-20 (RGR) package is product-preview.

PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V	5, 6, 7, 9, 10, 11	Output voltage setting pins. These pins should be connected to ground or left floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) when not in use. See the *ANY-OUT Programmable Output Voltage* section for more details.
BIAS	12	BIAS supply voltage pin for the use of 1.1 V ≤ V_{IN} ≤ 1.4 V and to connect a capacitor between this pin and ground.
EN	14	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. See the *Startup* section for more details.
FB	3	Output voltage feedback pin connected to the error amplifier. Although not required, a 10-nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended for low-noise applications to maximize ac performance. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
GND	8, 18	Ground pin
IN	15-17	Input supply voltage pin. A 10-µF input ceramic capacitor is required. See the *Input Capacitor Requirements* section for more details.
OUT	1, 19, 20	Regulated output pin. A 22-µF or larger ceramic capacitor is required for stability (a 10-µF minimum effective capacitance is required). See the *Output Capacitor Requirements* section for more details.
PG	4	Active-high power-good pin. An open-drain output indicates when the output voltage reaches 87% of the target. The use of a feed-forward capacitor may disrupt PG (power good) functionality. See the *Power-Good* section for more details.
SNS	2	Output voltage sense input pin. Connect this pin only if the ANY-OUT feature is used. See the *ANY-OUT Programmable Output Voltage* and *Adjustable Operation* sections for more details.
NR/SS	13	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a capacitor is recommended for low-noise applications to connect a 10-nF capacitor from NR/SS to GND (as close to the device as possible) to maximize ac performance. See the *Noise Reduction and Soft-Start* section for more details.
Thermal Pad	Pad	TI strongly recommends connecting the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 32R = 1.024 MΩ (that is, 1R = 3.2 kΩ).

Figure 1. Functional Block Diagram

TYPICAL CHARACTERISTICS

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

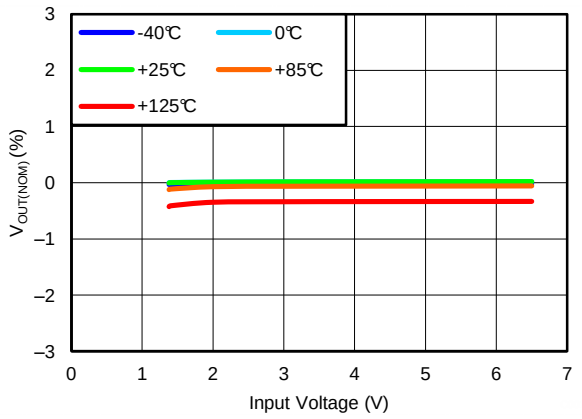


Figure 2. LINE REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, I_{OUT} = 5 mA, V_{BIAS} = Open)

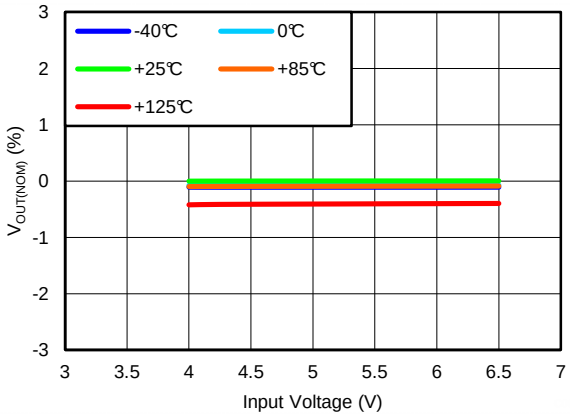


Figure 3. LINE REGULATION
($V_{OUT(TARGET)}$ = 3.95 V, ANY-OUT, I_{OUT} = 5 mA, V_{BIAS} = Open)

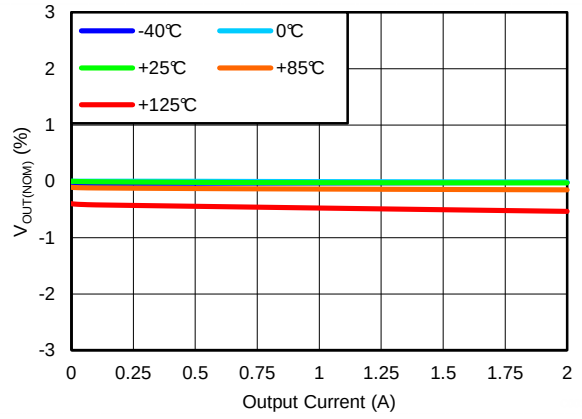


Figure 4. LOAD REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.4 V, V_{BIAS} = Open)

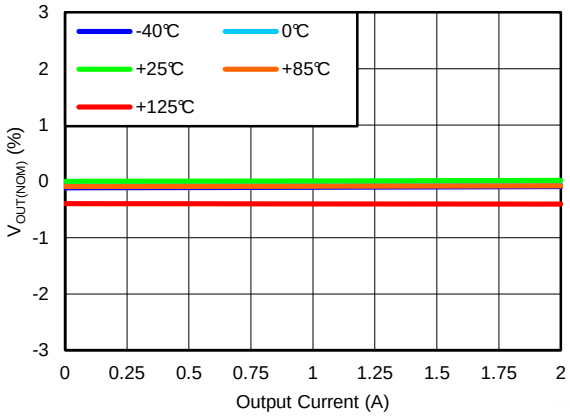


Figure 5. LOAD REGULATION
($V_{OUT(TARGET)}$ = 3.95 V, ANY-OUT, V_{IN} = 4.25 V, V_{BIAS} = Open)

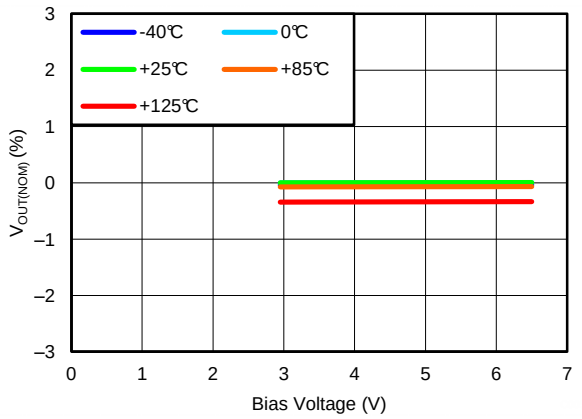


Figure 6. BIAS LINE REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V, I_{OUT} = 5 mA)

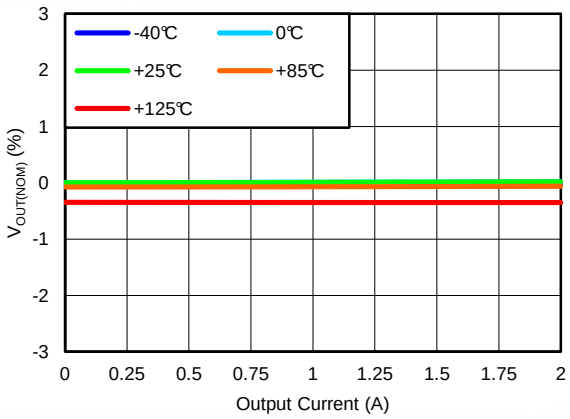


Figure 7. LOAD REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V, V_{BIAS} = 3 V)

(1) BIAS supply is required when the V_{IN} supply is below 1.4 V. Conversely, no BIAS supply is needed when the V_{IN} supply is higher than or equal to 1.4 V.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

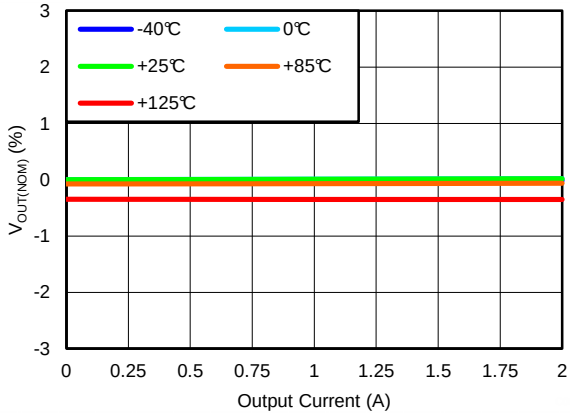


Figure 8. LOAD REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, Adjustable, V_{IN} = 1.1 V, V_{BIAS} = 6.5 V)

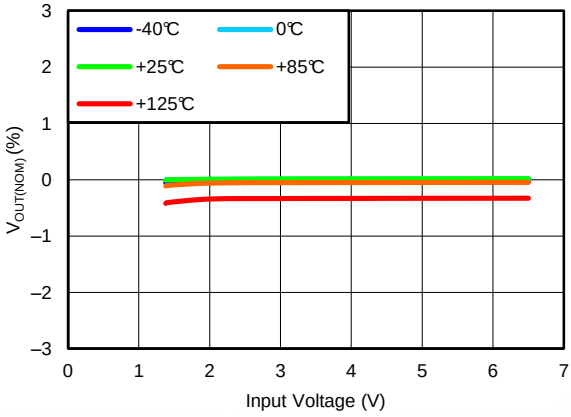


Figure 9. LINE REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, Adjustable, I_{OUT} = 5 mA, V_{BIAS} = Open)

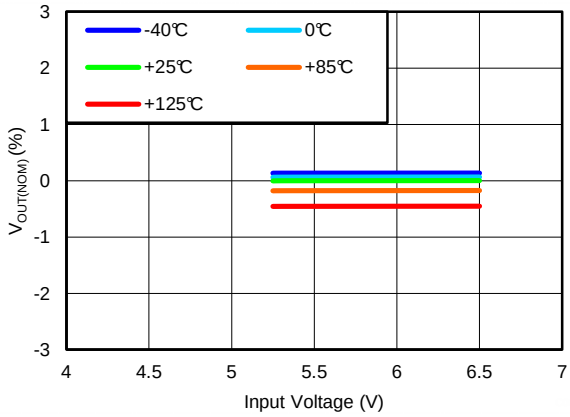


Figure 10. LINE REGULATION
($V_{OUT(TARGET)}$ = 5 V, Adjustable, I_{OUT} = 5 mA, V_{BIAS} = Open)

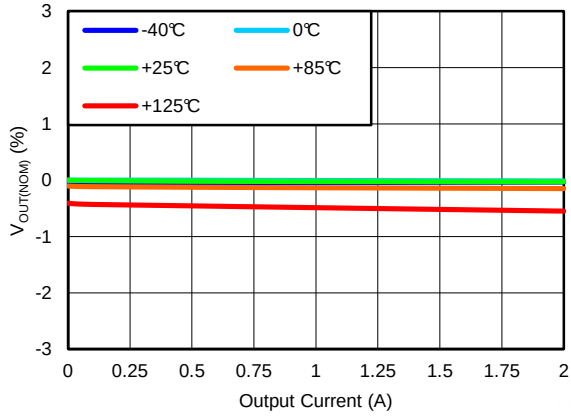


Figure 11. LOAD REGULATION
($V_{OUT(TARGET)}$ = 0.8 V, Adjustable, V_{IN} = 1.4 V, V_{BIAS} = Open)

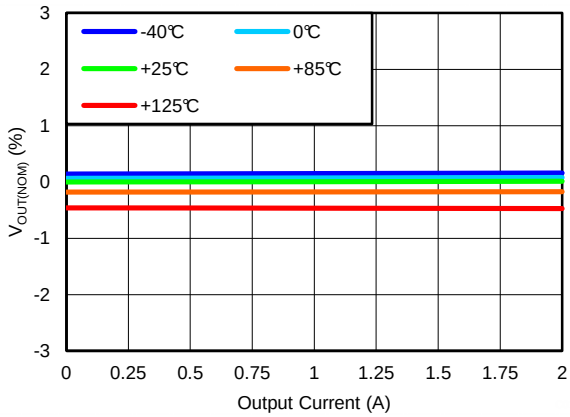


Figure 12. LOAD REGULATION
($V_{OUT(TARGET)}$ = 5 V, Adjustable, V_{IN} = 5.3 V, V_{BIAS} = Open)

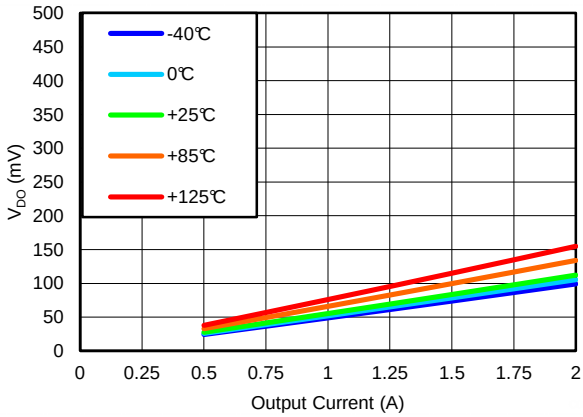


Figure 13. DROPOUT VOLTAGE vs OUTPUT CURRENT
(V_{IN} = 1.4 V V, ANY-OUT, V_{BIAS} = Open)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

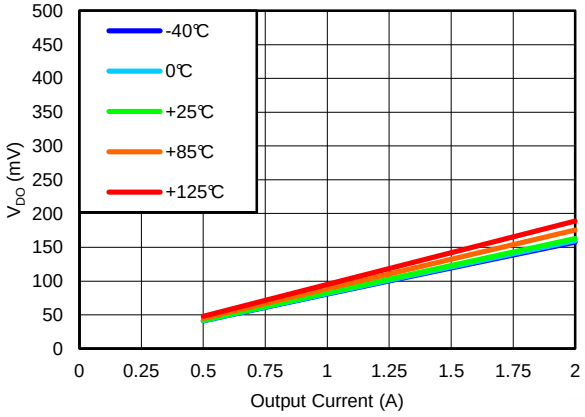


Figure 14. DROPOUT VOLTAGE vs OUTPUT CURRENT (V_{IN} = 5.5 V, ANY-OUT, V_{BIAS} = Open)

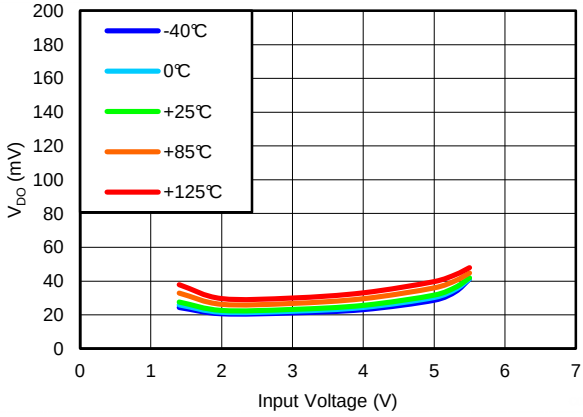


Figure 15. DROPOUT VOLTAGE vs INPUT VOLTAGE (I_{OUT} = 0.5 A, ANY-OUT, V_{BIAS} = Open)

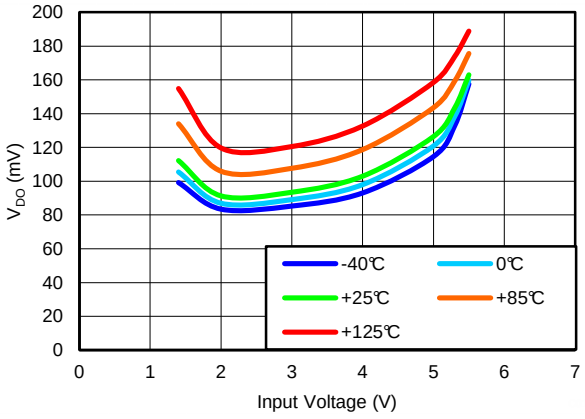


Figure 16. DROPOUT VOLTAGE vs INPUT VOLTAGE (I_{OUT} = 2 A, ANY-OUT, V_{BIAS} = Open)

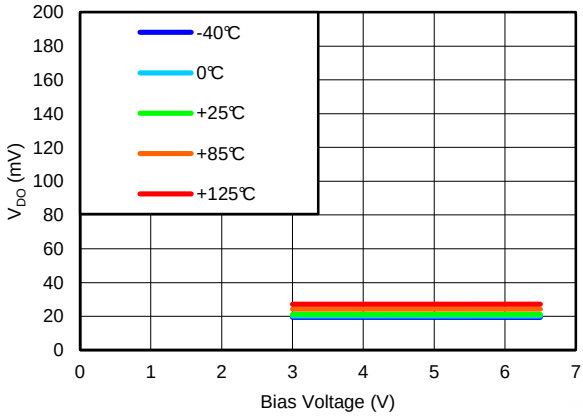


Figure 17. DROPOUT VOLTAGE vs BIAS VOLTAGE (I_{OUT} = 0.5 A, ANY-OUT, V_{IN} = 1.1 V)

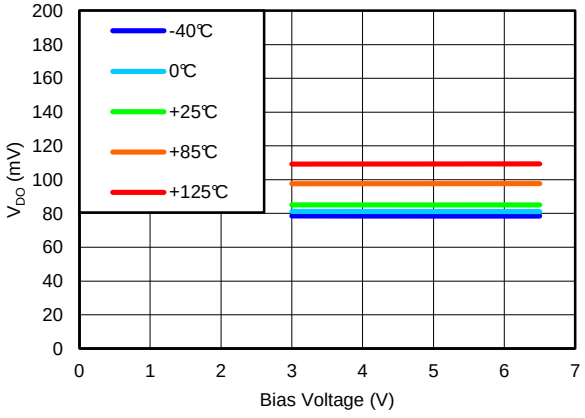


Figure 18. DROPOUT VOLTAGE vs BIAS VOLTAGE (I_{OUT} = 2 A, ANY-OUT, V_{IN} = 1.1 V)

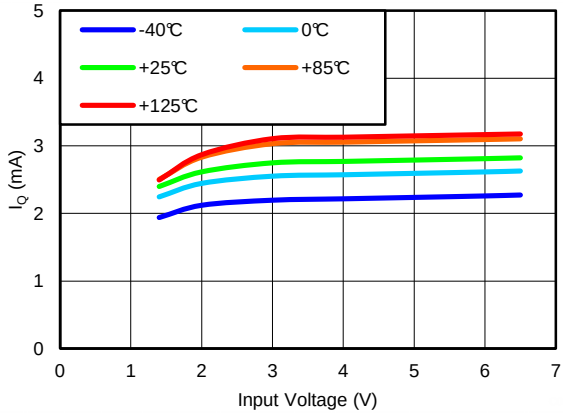


Figure 19. GROUND CURRENT vs INPUT VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, I_{OUT} = 5 mA, V_{BIAS} = Open)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

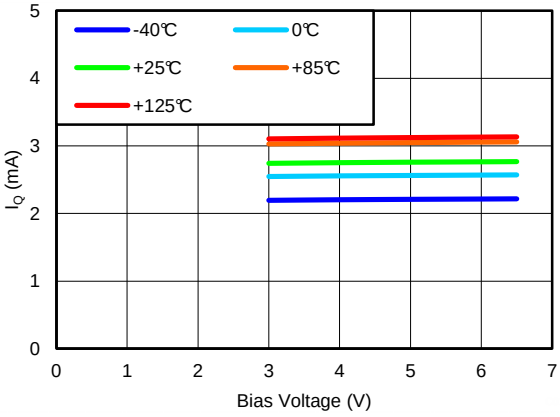


Figure 20. GROUND CURRENT vs BIAS VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, I_{OUT} = 5 mA, V_{IN} = 1.1 V)

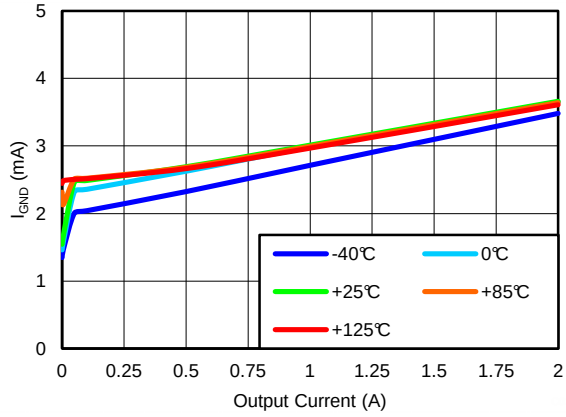


Figure 21. GROUND CURRENT vs OUTPUT CURRENT ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.4 V, V_{BIAS} = Open)

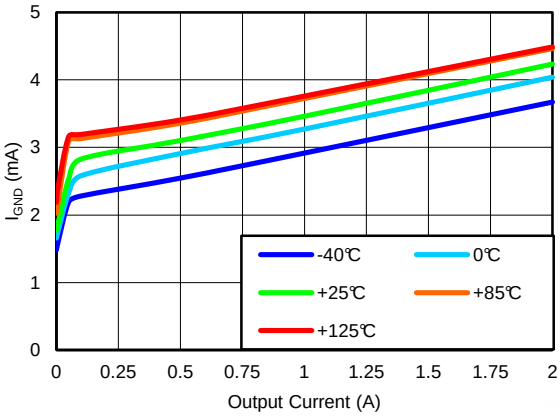


Figure 22. GROUND CURRENT vs OUTPUT CURRENT ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V, V_{BIAS} = 3 V)

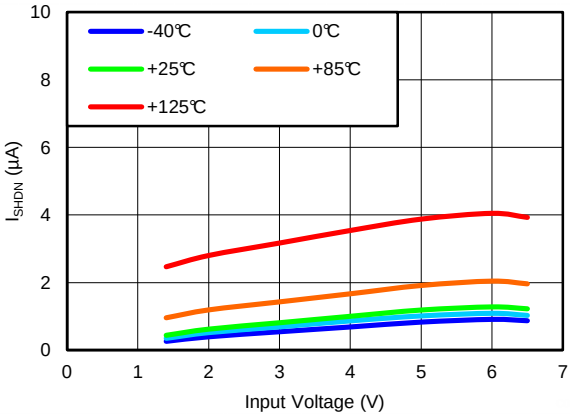


Figure 23. SHUTDOWN CURRENT vs INPUT VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{BIAS} = Open)

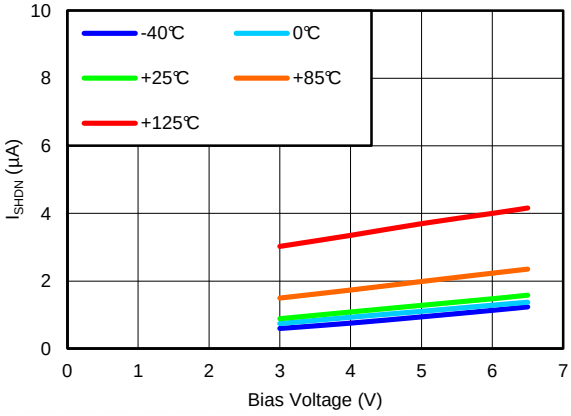


Figure 24. SHUTDOWN CURRENT vs BIAS VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V)

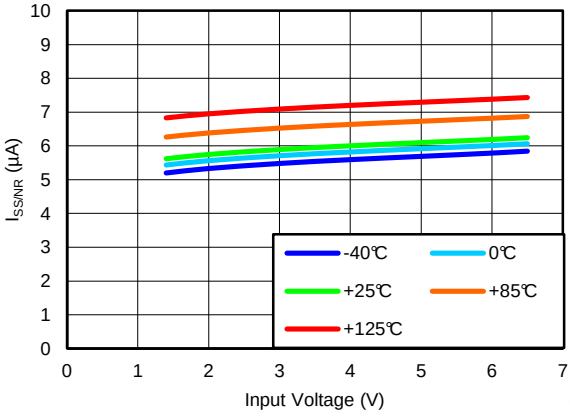


Figure 25. SOFT-START CURRENT vs INPUT VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{BIAS} = Open)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

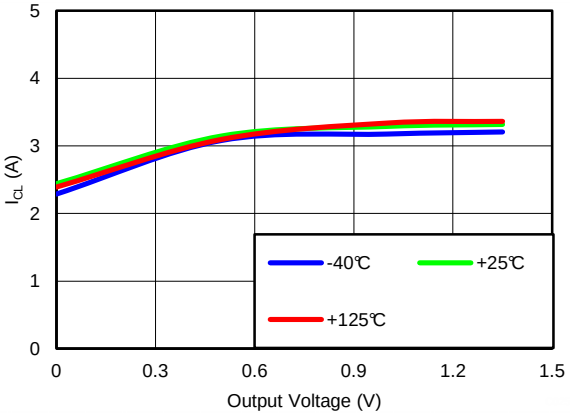


Figure 26. CURRENT LIMIT vs OUTPUT VOLTAGE ($V_{OUT(TARGET)}$ = 1.5 V, ANY-OUT, V_{IN} = 1.8 V, V_{BIAS} = Open)

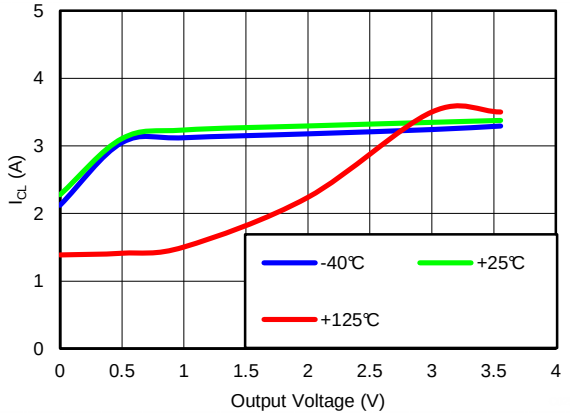


Figure 27. CURRENT LIMIT vs OUTPUT VOLTAGE ($V_{OUT(TARGET)}$ = 3.95 V, ANY-OUT, V_{IN} = 4.25 V, V_{BIAS} = Open)

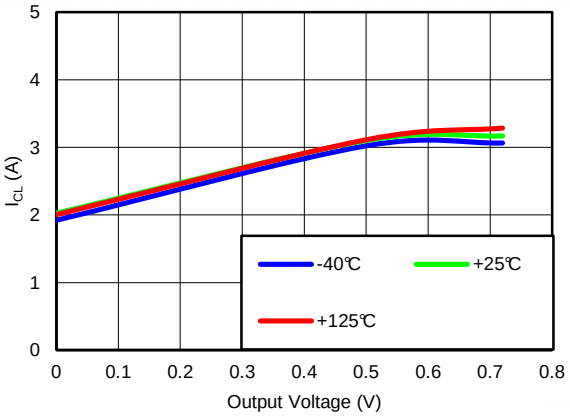


Figure 28. CURRENT LIMIT vs OUTPUT VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V, V_{BIAS} = 3 V)

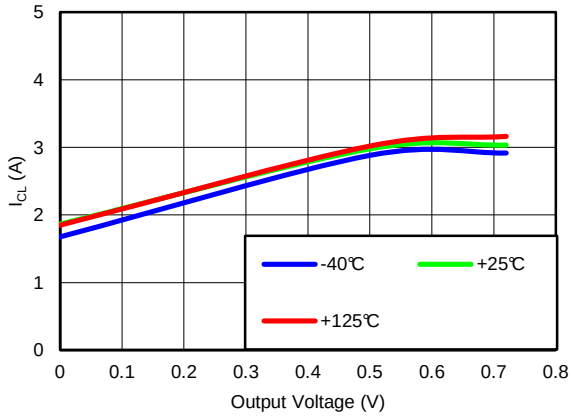


Figure 29. CURRENT LIMIT vs OUTPUT VOLTAGE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V, V_{BIAS} = 6.5 V)

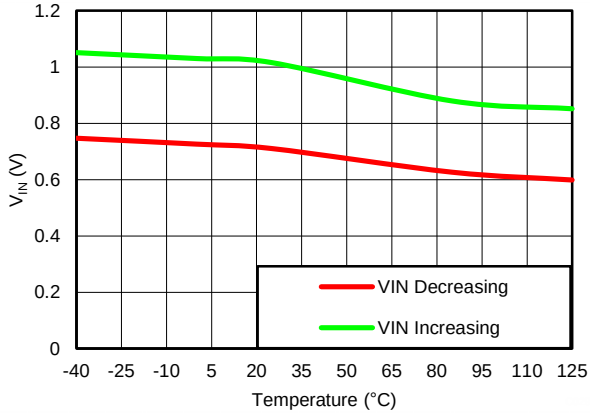


Figure 30. INPUT UVLO THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{BIAS} = 3.0 V)

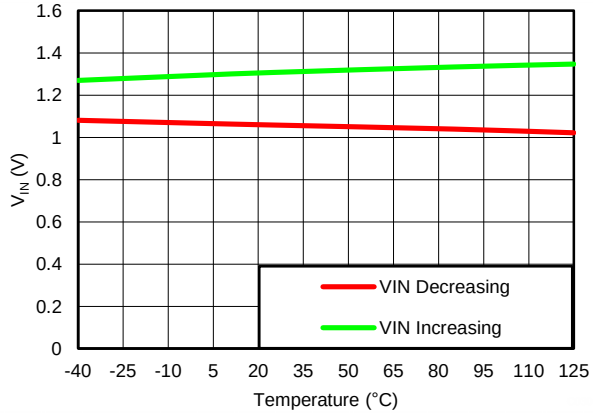


Figure 31. INPUT UVLO THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{BIAS} = Open)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

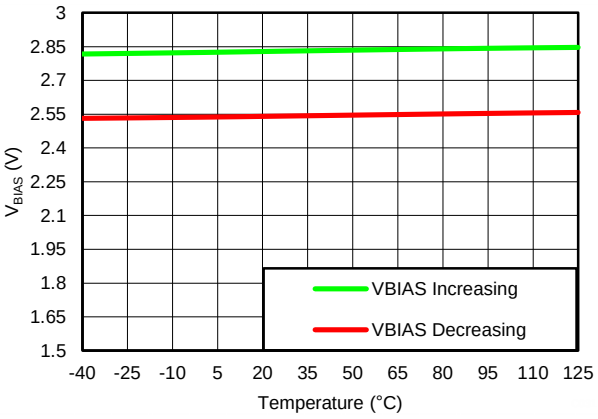


Figure 32. BIAS UVLO THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.1 V)

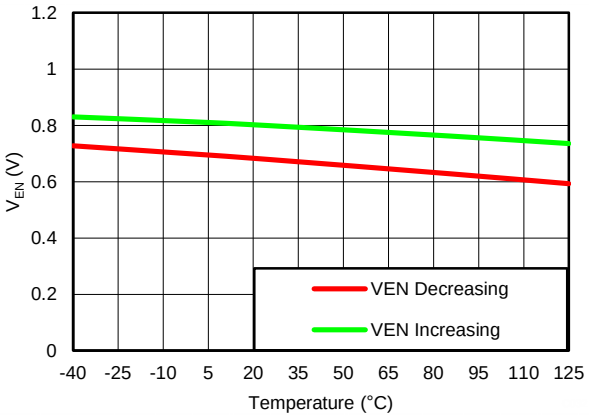


Figure 33. ENABLE THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.4 V, V_{BIAS} = Open)

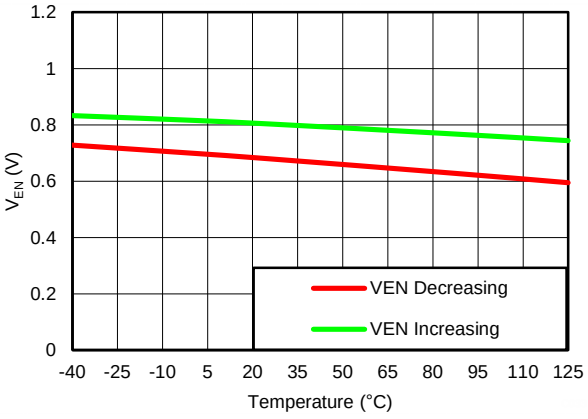


Figure 34. ENABLE THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 6.5 V, V_{BIAS} = Open)

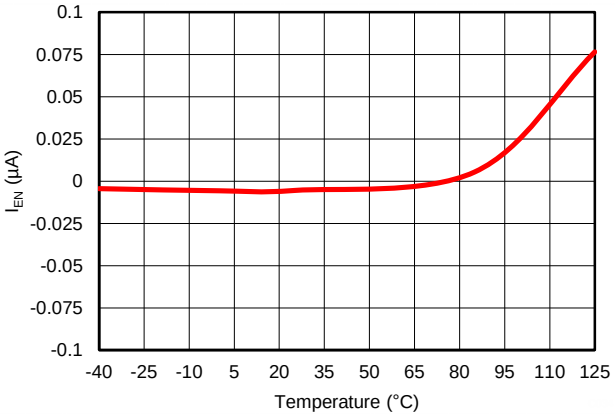


Figure 35. ENABLE CURRENT vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = V_{EN} = 6.5 V, V_{BIAS} = Open)

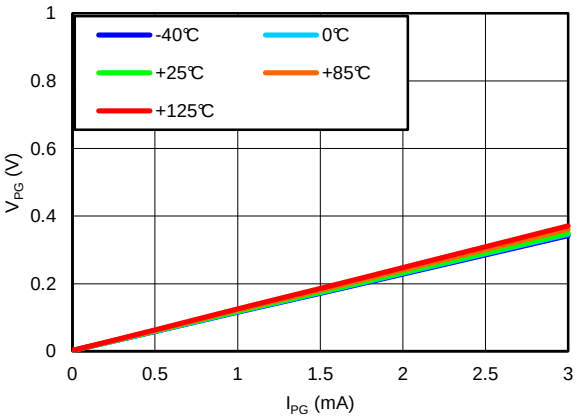


Figure 36. PG LOW VOLTAGE vs PG CURRENT ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 6.5 V, V_{BIAS} = Open)

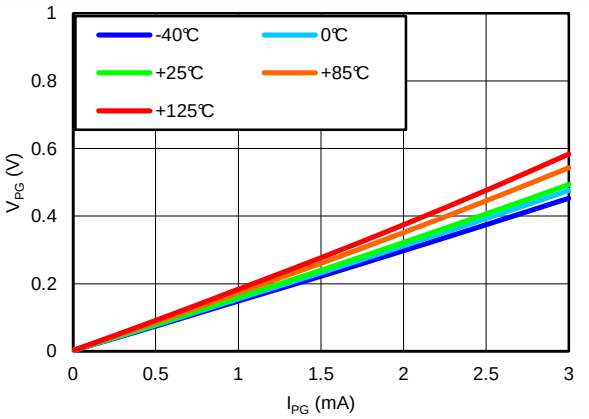


Figure 37. PG LOW VOLTAGE vs PG CURRENT ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.4 V, V_{BIAS} = Open)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

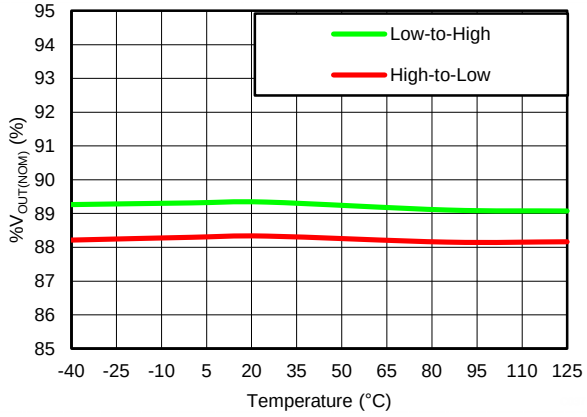


Figure 38. PG THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 6.5 V, V_{BIAS} = Open)

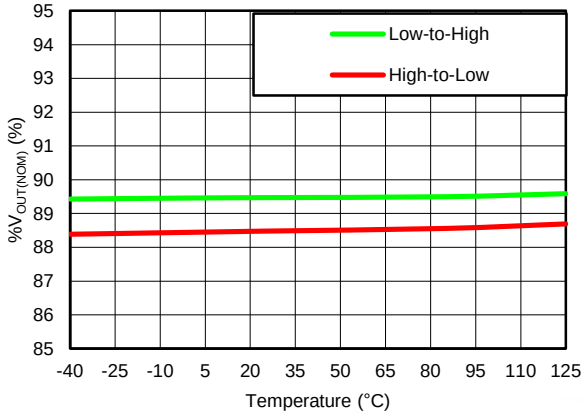


Figure 39. PG THRESHOLD vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = 1.4 V, V_{BIAS} = Open)

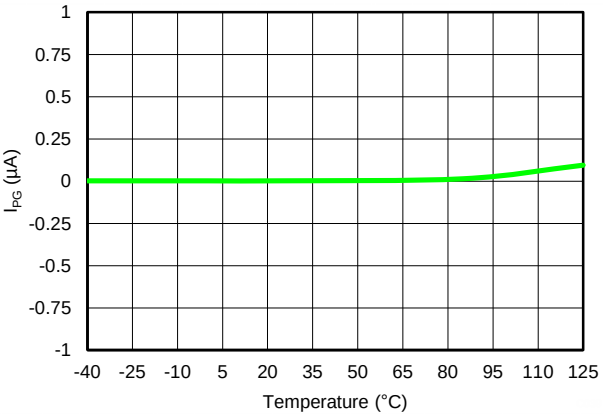


Figure 40. PG CURRENT vs TEMPERATURE ($V_{OUT(TARGET)}$ = 0.8 V, ANY-OUT, V_{IN} = V_{PG} = 6.5 V, V_{BIAS} = Open)

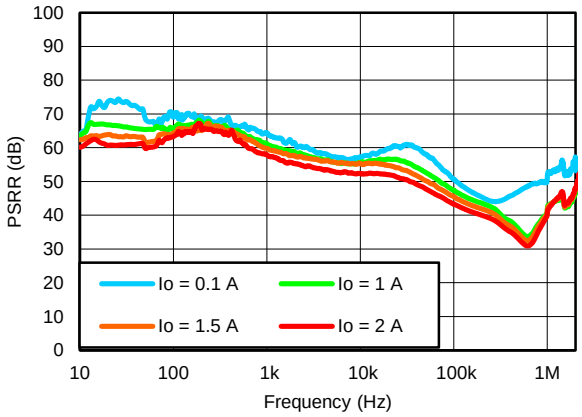


Figure 41. POWER-SUPPLY REJECTION vs CURRENT ($V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{IN} = V_{EN} = 3.8 V, V_{BIAS} = Open, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF)

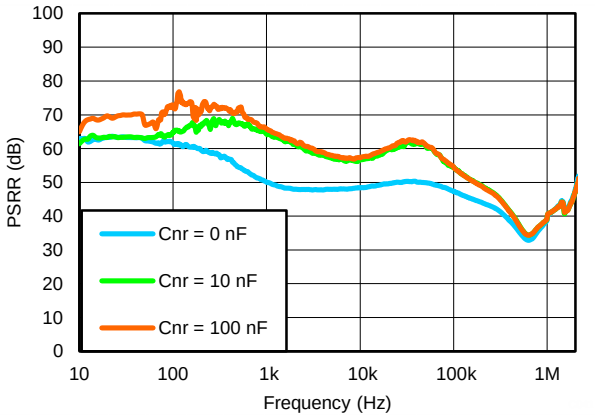


Figure 42. POWER-SUPPLY REJECTION vs $C_{NR/SS}$ ($V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{IN} = V_{EN} = 3.8 V, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, C_{FF} = 10 nF)

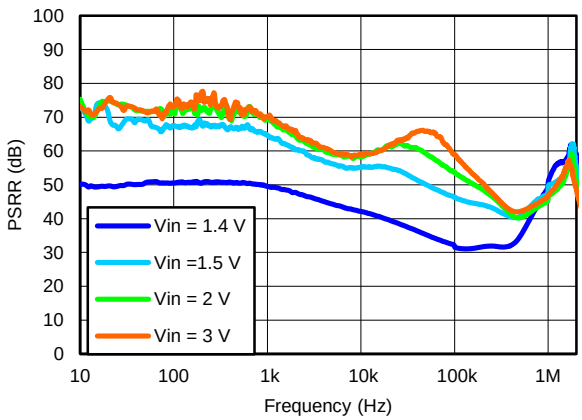


Figure 43. POWER-SUPPLY REJECTION vs INPUT VOLTAGE ($V_{OUT(TARGET)}$ = 1.2 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

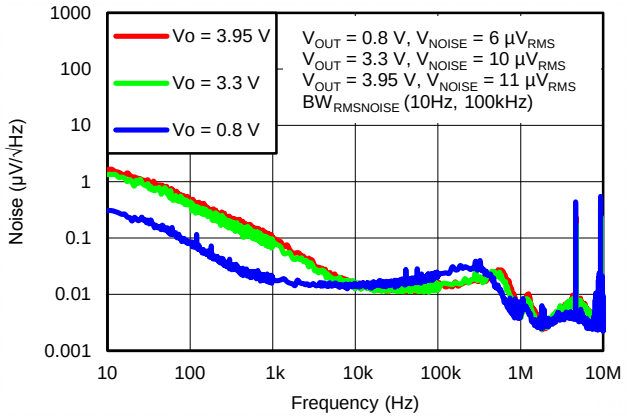


Figure 44. SPECTRAL NOISE DENSITY vs OUTPUT VOLTAGE (V_{IN} = $V_{OUT(TARGET)}$ + 0.5 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = C_{FF} = 10 nF)

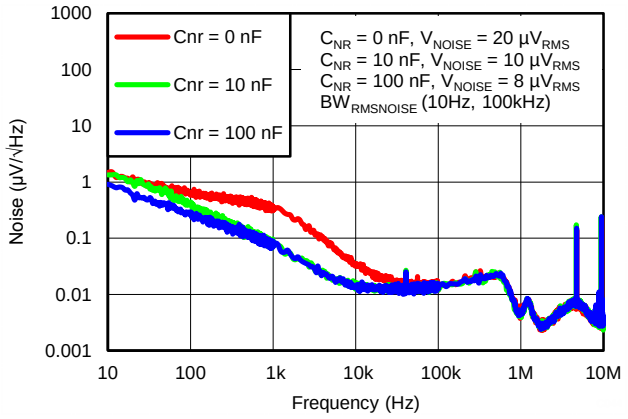


Figure 45. SPECTRAL NOISE DENSITY vs $C_{NR/SS}$ (V_{IN} = 3.8 V, $V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, C_{FF} = 10 nF)

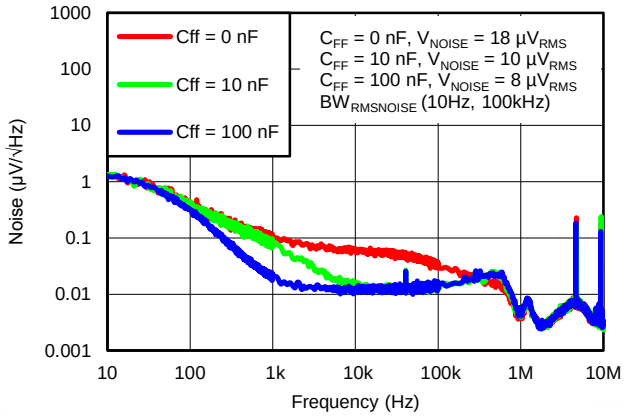


Figure 46. SPECTRAL NOISE DENSITY vs $C_{SS/NR}$ (V_{IN} = 3.8 V, $V_{OUT(TARGET)}$ = 3.3 V, ANY-OUT, V_{BIAS} = Open, I_{OUT} = 1.5 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF)

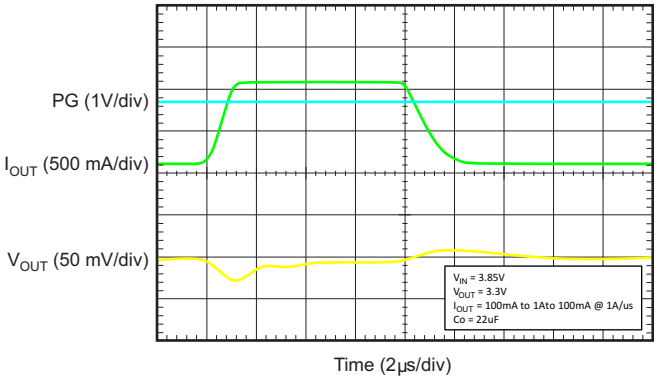


Figure 47. LOAD TRANSIENT RESPONSE

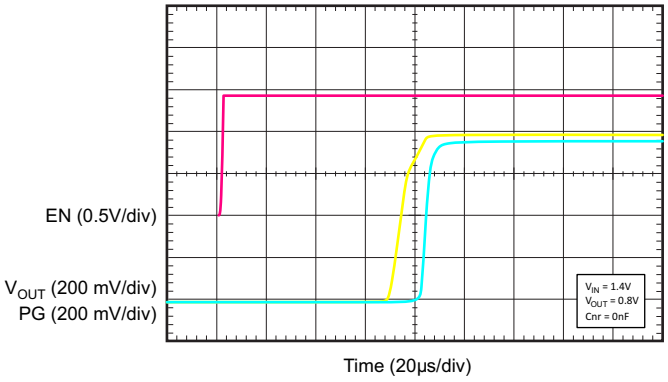


Figure 48. START-UP (C_{NR} = 0 nF)

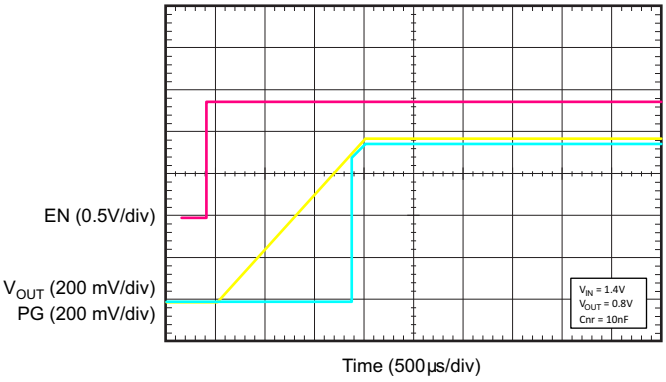


Figure 49. START-UP (C_{NR} = 10 nF)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, {1.1 V ≤ V_{IN} < 1.4 V and 3.0 V ≤ V_{BIAS} ≤ 6.5 V} or {V_{IN} ≥ 1.4 V and V_{BIAS} open}(1), V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3 V, $V_{OUT(TARGET)}$ = 0.8 V, OUT connected to 50 Ω to GND, V_{EN} = 1.1 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 10 nF, and PG pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

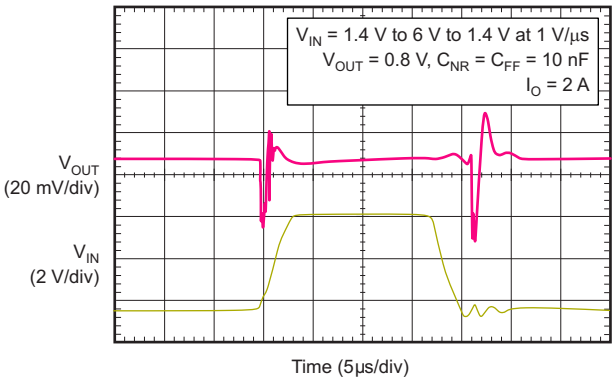


Figure 50. LINE TRANSIENT

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUIT

Output voltage is set by grounding the appropriate control pins, as shown in Figure 51. When grounded, all control pins add a specific voltage on top of the internal reference voltage (V_{REF} = 0.8 V).

For example, when grounding the 400-mV pin, the voltage value of 400 mV is added to the 0.8-V internal reference voltage for $V_{OUT(NOM)}$ equal to 1.2 V; alternatively, when grounding the 200 mV pin, the voltage value of 200 mV is added to the 0.8-V internal reference voltage for $V_{OUT(NOM)}$ equal to 1.0 V, as described in Equation 1 and Equation 2.

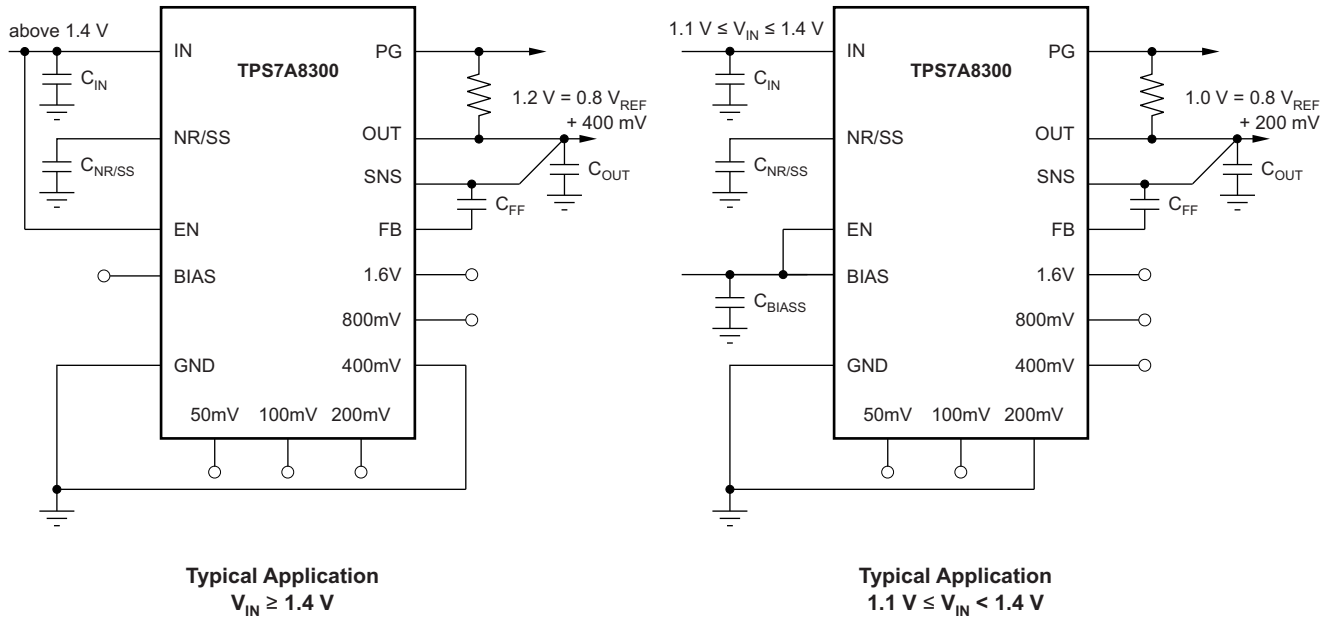


Figure 51. Maximize PSRR Performance and Minimize RMS Noise

$$V_{OUT(NOM)} = V_{REF} + 0.4\ V = 0.8\ V + 0.4\ V = 1.2\ V \quad (1)$$

$$V_{OUT(NOM)} = V_{REF} + 0.2\ V = 0.8\ V + 0.2\ V = 1.0\ V \quad (2)$$

ANY-OUT PROGRAMMABLE OUTPUT VOLTAGE

The TPS7A8300 does not require external resistors to set output voltage, which is typical of low-dropout voltage regulators (LDOs), but uses device pins 5, 6, 7, 9, 10, and 11 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open (or floating). ANY-OUT programming is set by Equation 3 as the sum of the internal reference voltage (V_{REF} = 0.8 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 50 mV (pin 5), 100 mV (pin 6), 200 mV (pin 7), 400 mV (pin 9), 800 mV (pin 10), or 1.6 V (pin 11). Table 1 summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF}.

$$V_{OUT} = V_{REF} + (\Sigma\ \text{ANY-OUT Pins to Ground}) \quad (3)$$

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5 (50 mV)	50 mV
Pin 6 (100 mV)	100 mV
Pin 7 (200 mV)	200 mV
Pin 9 (400 mV)	400 mV
Pin 10 (800 mV)	800 mV
Pin 11 (1.6 V)	1.6 V

Table 2 shows a full list of target output voltages and corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 0.8 V to 3.95 V in 50-mV steps.

There are several alternative ways to set the output voltage. The program pins can be driven using external general-purpose input/output pins (GPIOs), manually connected to ground using 0-Ω resistors (or left open), or hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage.

NOTE

For output voltages greater than 3.95 V, use a traditional adjustable configuration (see the *Adjustable Operation* section).

Table 2. User-Configurable Output Voltage Settings

$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V	$V_{OUT(TARGET)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

ADJUSTABLE OPERATION

The adjustable version of the device has an output voltage range of 0.8 V to 5 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 52.

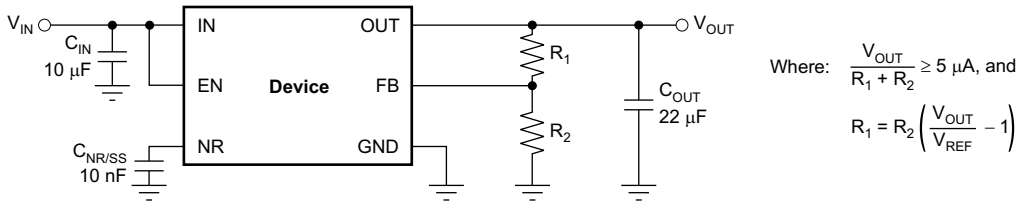


Figure 52. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using Equation 4. This resistive network must provide a current equal to or greater than 5 µA for optimum noise performance.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\ \mu A \tag{4}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

Table 3 shows the resistor combination needed to achieve a few of the most common rails using commercially-available, 0.1%-tolerance resistors to maximize nominal voltage accuracy while abiding to the formula shown in Equation 4.

Table 3. Recommended Feedback-Resistor Values

$V_{OUT(TARGET)}$ (V)	FEEDBACK RESISTOR VALUES(1)	
	R_1 (kΩ)	R_2 (kΩ)
1.00	2.55	10.2
1.20	5.9	11.8
1.50	9.31	10.7
1.80	18.7	15
1.90	15.8	11.5
2.50	24.3	11.5
3.00	31.6	11.5
3.30	35.7	11.5
5.00	105	20

(1) R_1 is connected from OUT to FB; R_2 is connected from FB to GND.

CAPACITOR RECOMMENDATION

The TPS7A8300 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and at the noise-reduction pin (NR, pin 13). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and temperature and the design engineer should be aware of these characteristics. As a rule of thumb, ceramic capacitors are recommended to be derated by 50%. To compensate for this derating, increase capacitor size by 100%. The input and output capacitors recommended herein account for a capacitance derating of 50%.

Attention should be given to the input capacitance to minimize transient input droop during load current steps. Input capacitances of 10 µF or greater provide the desired effect and do not affect stability. However, note that simply using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor (in combination with the wire-lead inductance) creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10-µF input capacitor form an LC filter with a resonance frequency of 712 kHz that is near the edge of the control loop bandwidth. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A8300 is designed and characterized for operation with ceramic capacitors of 22 µF or greater at the output and 10 µF at the input. Note especially that input and output capacitances should be located as near as practical to the respective input and output pins.

Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The TPS7A8300 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$).This soft-start eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic start-up, the TPS7A8300 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Soft-start ramp time can be calculated with Equation 5.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (5)$$

For low-noise applications, the noise-reduction capacitor (connected to the NR/SS pin of the LDO) forms an RC filter for filtering out noise that might ordinarily be amplified by the control loop and appear on the output voltage. For low-noise applications, a 10-nF to 1-µF $C_{NR/SS}$ is recommended.

Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, TI recommends using a 10-nF feed-forward capacitor in low-noise applications to maximize ac performance.

INTERNAL CURRENT LIMIT (I_{CL})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate at a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls while load impedance decreases. Note also that when a current limit occurs while the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high, the device may not start up. In applications that function with both a positive and negative voltage supply, there are several ways to ensure proper start-up:

- The TPS7A8300 should be enabled first and disabled last.
- Delaying the EN voltage with respect to IN voltage allows the internal pull-down resistor to discharge any residual voltage at OUT. If a faster discharge rate is required, an external resistor from OUT to GND may be used.

DROPOUT VOLTAGE (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$). However, in the Electrical Characteristics, V_{DO} is defined as the $V_{IN} – V_{OUT}$ voltage at the rated current (I_{RATED}), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(ON)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then the V_{DO} for that current scales accordingly. The $R_{DS(ON)}$ for the TPS7A8300 can be calculated using Equation 6:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (6)$$

OUTPUT VOLTAGE ACCURACY

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error typically includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the Electrical Characteristics. Output voltage accuracy also accounts for all variations between manufacturing lots.

POWER-GOOD FUNCTION

The TPS7A8300 has a power-good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage ($V_{IT(PG)}$), the PG pin open-drain output engages (low impedance to GND). When the output voltage exceeds the $V_{IT(PG)}$ threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high-impedance. By connecting a pull-up resistor to an external supply, any downstream device can receive PG as a logic signal. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices. Use a pull-up resistor from 10 kΩ to 100 kΩ.

The power-good function is not valid when employing the feed-forward capacitor (C_{FF}).

START-UP

Enable (EN) and Undervoltage Lockout (UVLO)

The TPS7A8300 only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input and bias voltage (V_{IN} and V_{BIAS}, respectively) to prevent device turn-on before V_{IN} and V_{BIAS} rises above the lockout voltage. The UVLO circuit also causes a shutdown when V_{IN} and V_{BIAS} falls below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. EN can be connected directly to V_{IN} if independent turn-on is not needed.

Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO have achieved threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current into the LDO at the IN pin during the time of the turn-on ramp up. Inrush current then consists primarily of the sum of load and charge current to the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, this soft-start current can be estimated by Equation 7:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (7)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp,
- $dV_{OUT}(t)/dt$ is the slope of the V_{OUT} ramp, and
- R_{LOAD} is the resistive load impedance.

AC PERFORMANCE

LDO ac performance is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

Power-Supply Ripple Rejection (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Even though PSRR is therefore a loss in noise signal amplitude (the output ripple relative to the input ripple), the PSRR reciprocal is plotted in the Electrical Characteristics as a positive number in decibels (dB) for convenience. Equation 8 gives the PSRR calculation as a function of frequency where input noise voltage [$V_{S(IN)}(f)$] and output noise voltage [$V_{S(OUT)}(f)$] are understood to be purely ac signals.

$$PSRR\ (dB) = 20\ Log_{10}\left[\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)}\right] \tag{8}$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise-reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for optimal PSRR.

The LDO is often employed not only as a dc-dc regulator, but also to provide exceptionally clean power-supply voltages that are free of noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A8300.

Load-Step Transient Response

The load-step transient response is the output voltage response by the LDO to a step change in load current, whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 2 A (at 1 A per microsecond) and shows a classic critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers as the control loop adjusts itself. The depth of charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, recovery speed is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case off-loading step characterization occurs when the current step transitions from 2 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. Because the LDO cannot sink charge current, the control loop must turn off the main pass-FET to wait for the charge to deplete, thus giving the off-load step its typical monotonic decay (which appears triangular in shape).

Noise

The TPS7A8300 is designed, in particular, for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits (for instance, where minimum phase noise is all important), or in-test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy.

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shut noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker noise, or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu V/\sqrt{Hz}$). RMS noise is then calculated in the usual manner as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

Behavior when transitioning from steady dropout into regulation

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, right after being in a normal regulation state, but *not* during startup), the pass device is driven as hard as possible, while the control loop is out of balance. During the normal time it takes the device to regain regulation, $V_{IN} \geq V_{OUT(NOM)} + V_{DO}$, V_{OUT} overshoots if the input voltage slew rate is 0.1 V/µs or faster.

THERMAL INFORMATION

Thermal Protection

The TPS7A8300 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds +160°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to +140°C (typical). The thermal time-constant of the semiconductor die is fairly short, and thus the output oscillates on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, the junction temperature should be limited to a maximum of +125°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown should occur at least +45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A8300 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A8300 into thermal shutdown degrades device reliability.

Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator should be as free as possible of other heat-generating devices that can cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. P_D can be calculated using Equation 9:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (9)$$

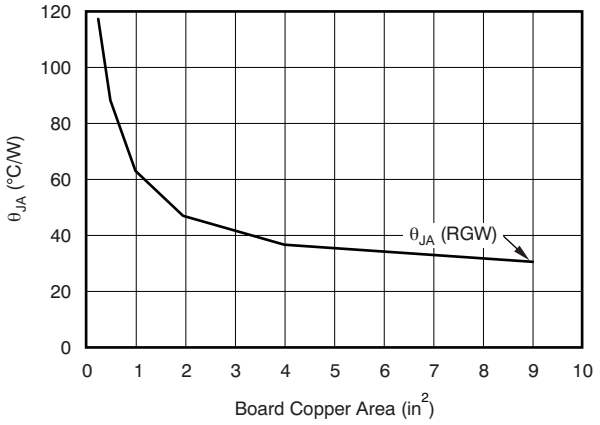
An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the QFN (RGW) package is through the thermal pad to the PCB. The thermal pad should be soldered to a copper pad area under the device. This pad area should then contain an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 10.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (10)$$

Unfortunately, this thermal resistance (θ_{JA}) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The θ_{JA} recorded in the Thermal Information table is determined by the JEDEC standard, PCB, and copper-spreading area and is to be used only as a relative measure of package thermal performance. Note that for a well-designed thermal layout, θ_{JA} is actually the sum of the QFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. When θ_{JCbot} is known, one can estimate the amount of heat-sinking area required for a given θ_{JA}, refer to Figure 53. θ_{JCbot} can be found in the Thermal Information table.



NOTE: θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 53. θ_{JA} vs Board Size

Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO while in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the Thermal Information table and are used in accordance with Equation 11.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in Equation 9,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (11)

BOARD LAYOUT

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and should be either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD™. In most applications, this ground plane is necessary to meet thermal requirements.

REVISION HISTORY

NOTE: Page numbers for previous revision may differ from page numbers in the current version.

Changes from Revision B (July 2013) to Revision C **Page**

- Changed text in *Feed-Forward Capacitor* subsection 19
- Changed *Power-Good* section 20
- Deleted *PG Functionality* section 20

Changes from Revision A (June 2013) to Revision B **Page**

- Changed from product preview to production data 1

Changes from Original (May 2013) to Revision A **Page**

- Changed product preview data sheet 1

PACKAGE OPTION ADDENDUM

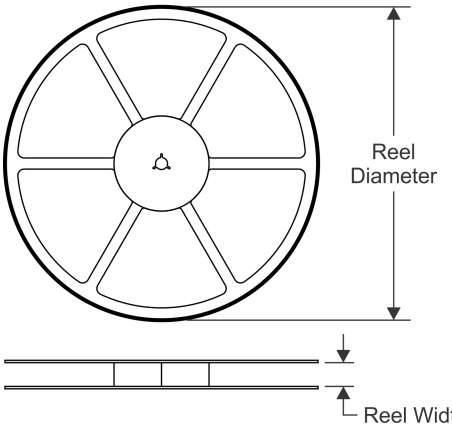
26-Aug-2013

PACKAGING INFORMATION

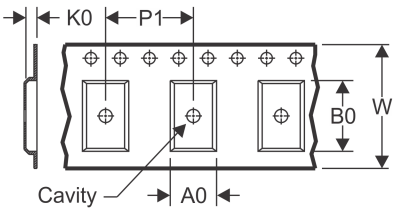
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A8300RGRR	PREVIEW	VQFN	RGR	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PA9Q	
TPS7A8300RGRT	PREVIEW	VQFN	RGR	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PA9Q	
TPS7A8300RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PZGM	Samples
TPS7A8300RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PZGM	Samples

TAPE AND REEL INFORMATION

REEL DIMENSIONS

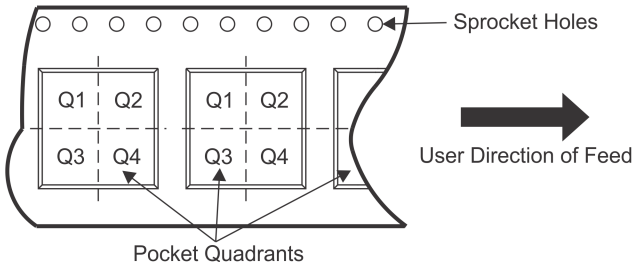


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



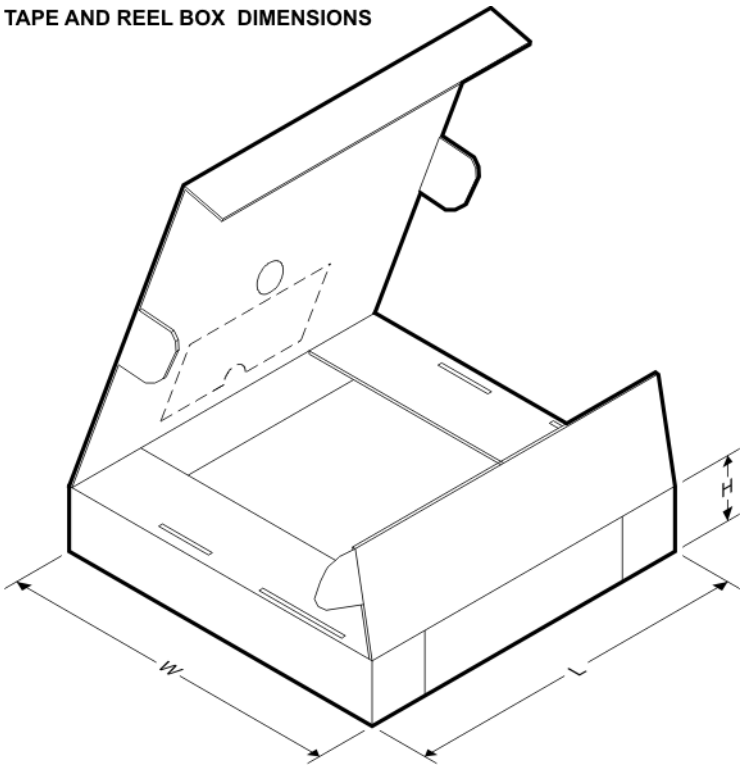
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8300RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

13-Aug-2013

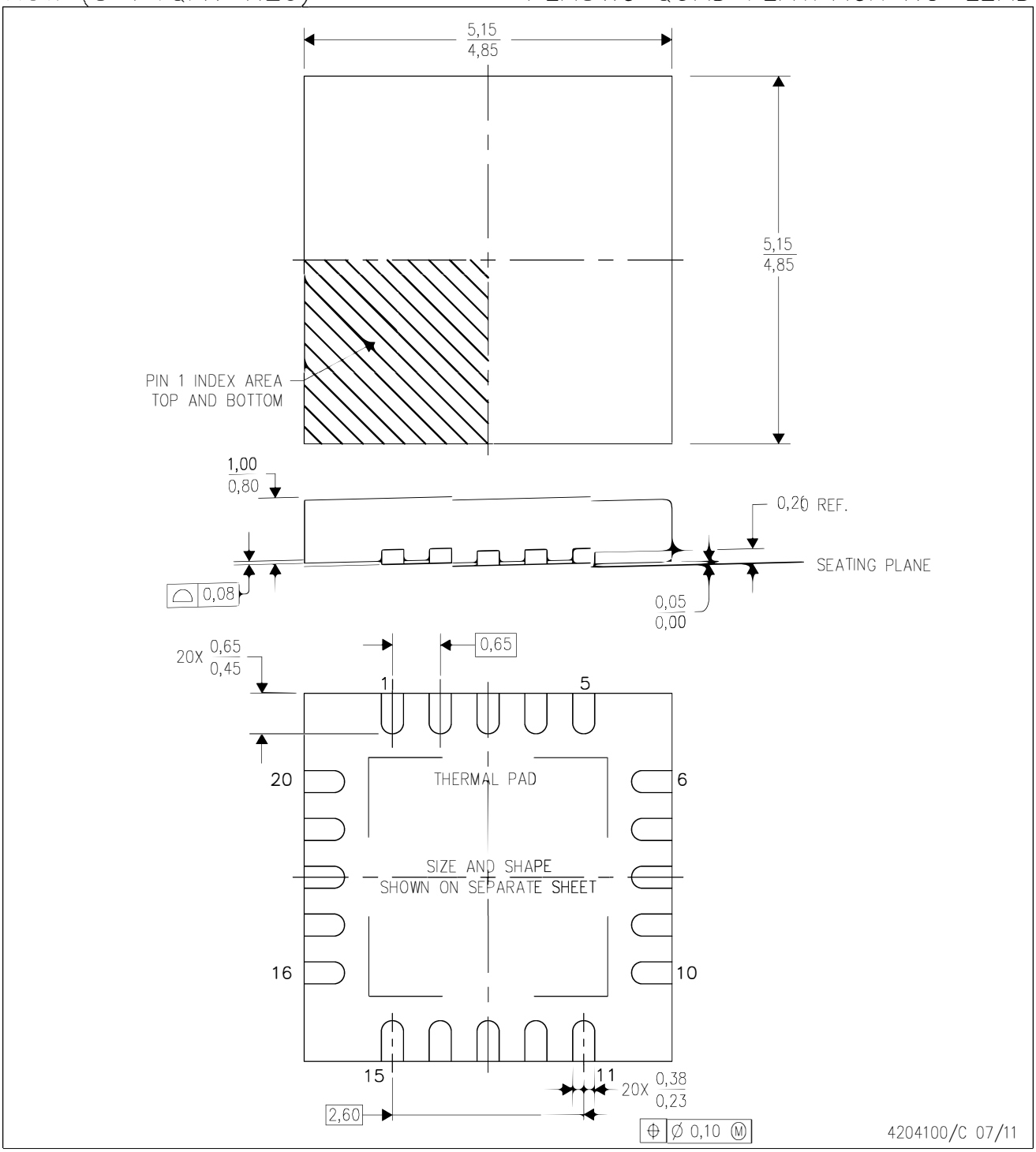
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8300RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

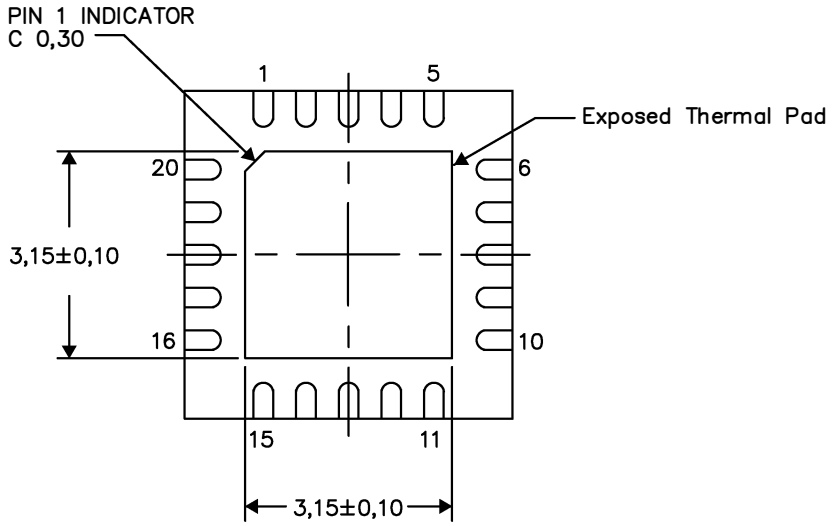
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



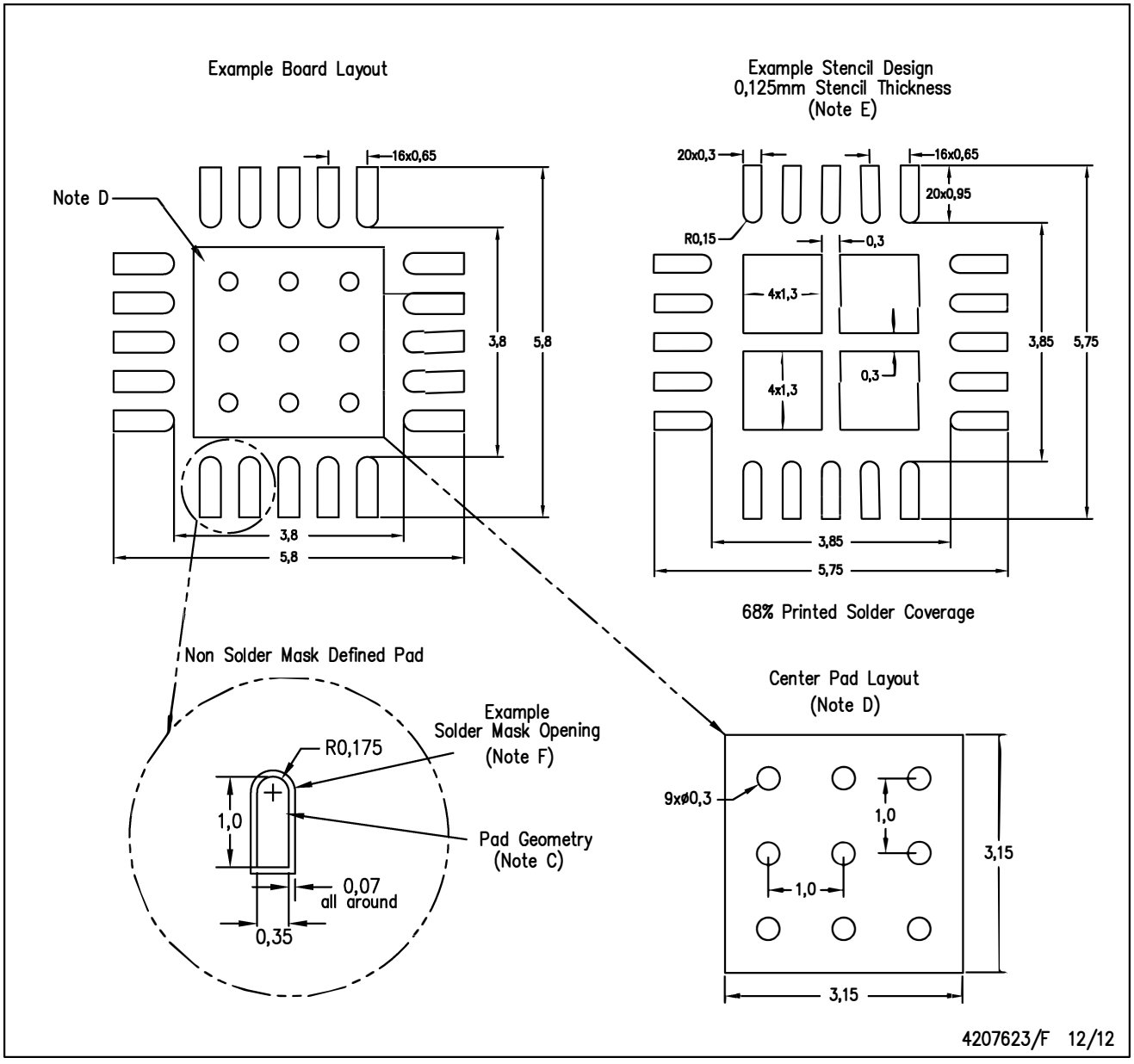
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

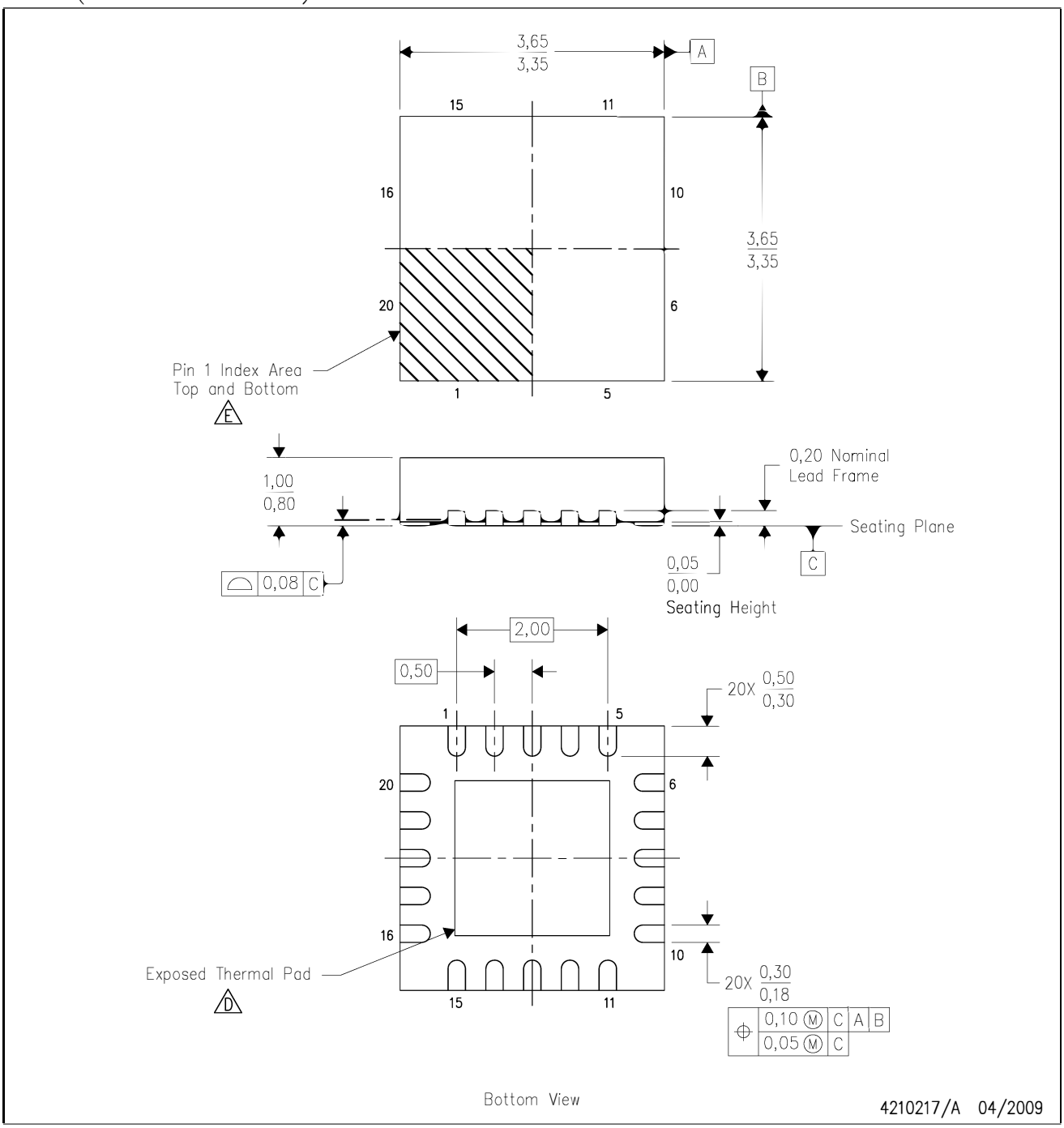
NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

RGR (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.