# TMUX154E ESD-Protected, Low Capacitance, 2-Channel, 2:1 Switch, With Powered-off Protection

## 1 Features

- $V_{CC}$ Operation at 3 V to 4.3 V
- I/O Pins Can Tolerate up to 5.25 V
- 1.8-V Compatible Control Logic
- Supports Powered-off Protection I/O Pins Hi-Z When $V_{CC}$ = 0 V
- $R_{ON}$ = 10 Ω Maximum
- $\Delta R_{ON}$ = 0.35 Ω Typical
- $C_{io(ON)}$ = 7.5 pF Typical
- Low Power Consumption (1 uA Maximum)
- –3-dB Bandwidth = 900 MHz Typical
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II (1)
- ESD Performance Tested Per JESD 22
  - 8000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O Port to GND (2)
  - 15000-V Human-Body Model

(1) Except $\overline{EN}$ and SEL Inputs
(2) High-voltage HBM is performed in addition to the standard HBM testing (A114-B, Class II) and applies to I/O ports tested with respect to GND only.

## 2 Applications

- Portable Electronics
- Printers and other Peripherals
- Electronic Point of Sale
- Building Automation
- Servers

## 3 Description

The TMUX154E is a high-bandwidth 2:1 switch specially designed for the switching of high-speed signals in applications with limited I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

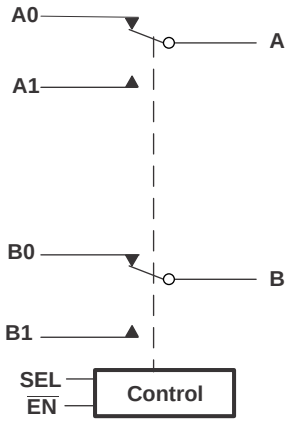
The TMUX154E integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.8 mm × 1.4 mm) or a VSSOP package, and is characterized over the free-air temperature range of –40°C to 85°C.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMUX154E | VSSOP (10) | 3.00 mm × 3.00 mm |
| | UQFN (10) | 1.80 mm × 1.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Functional Block Diagram**



# Table of Contents



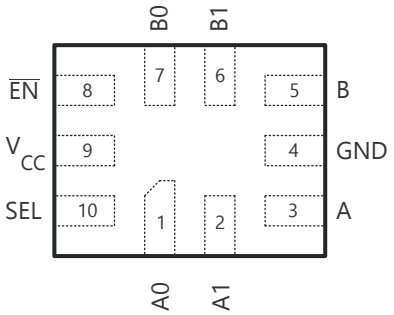
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

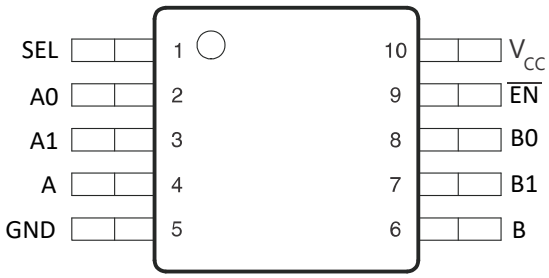
| DATE | REVISION | NOTES |
|---|---|---|
| February 2018 | * | Initial release. |

# 5 Pin Configuration and Functions

**RSW Package**
**10-PIN UQFN**
**Top View**




**DGS Package**
**10-PIN VSSOP**
**Top View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | UQFN | VSSOP | | |
| A0 | 1 | 2 | I/O | signal path port 0 |
| B0 | 7 | 8 | I/O | |
| A | 3 | 4 | I/O | Common signal path |
| B | 5 | 6 | I/O | |
| A1 | 2 | 3 | I/O | signal path port 1 |
| B1 | 6 | 7 | I/O | |
| $\overline{EN}$ | 8 | 9 | I | EN = 0 Enable<br>EN = 1 Disable |
| SEL | 10 | 1 | I | Select input:<br>SEL = 0 A,B to A0,B0<br>SEL = 1 A,B to A1,B1 |
| GND | 4 | 5 | — | Ground |
| VCC | 9 | 10 | — | Voltage supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1) (2))

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_{SEL}$, $V_{\overline{EN}}$ | Control input voltage | | –0.5 | 7 | V |
| $V_{I/O}$ | Signal path I/O voltage | $V_{CC}$ > 0 | –0.5 | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ = 0 | –0.5 | 5.25 | |
| $I_{IK}$ | Control input clamp current | $V_{IN}$ < 0 | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O}$ < 0 | | –50 | mA |
| $I_{I/O}$ | ON-state switch current | | | ±64 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | All pins | ±8000 | V |
| | | | I/O port to GND | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

See (1).

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 4.3 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 3 V to 3.6 V | 1.3 | $V_{CC}$ | V |
| | | $V_{CC}$ = 4.3 V | 1.7 | $V_{CC}$ | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 3 V to 3.6 V | 0 | 0.5 | V |
| | | $V_{CC}$ = 4.3 V | 0 | 0.7 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating ambient temperature | | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TMUX154E | | UNIT |
|---|---|---|---|---|
| | | DGS (VSSOP) | RSW (UQFN) | |
| | | 10 PINS | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 203.1 | 114.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 88.7 | 64.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 123.0 | 21.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.2 | 1.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 121.6 | 21.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

| PARAMETER | | TEST CONDITIONS | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SEL}$ , $I_{EN}$ | Control inputs | $V_{CC}$ = 4.3 V, 0 V, $V_{SEL}$,$V_{EN}$ = 0 to 4.3 V | | | ±1 | µA |
| $I_{OZ}$ | OFF-state leakage current[3] | $V_{CC}$ = 4.3 V, $V_O$ = 0 to 3.6 V, $V_I$ = 0, Switch OFF | | | ±1 | µA |
| $I_{OFF}$ | Powered off leakage current | $V_{CC}$ = 0 V, $V_{An,Bn}$ = 0 V, $V_{A,B}$ = 0 V to 4.3 V, $V_{SEL}$ , $V_{EN}$ = $V_{CC}$ or GND | | | ±2 | µA |
| $I_{CC}$ | Supply current | $V_{CC}$ = 4.3 V, $I_{I/O}$ = 0, Switch ON or OFF | | | 1 | µA |
| $\Delta I_{CC}$ [4] | Difference of supply current due to control input voltage not $V_{CC}$ or GND | $V_{CC}$ = 4.3 V, $V_{SEL}V_{EN}$ = 2.6 V | | | 10 | µA |
| $C_{SEL}$, $C_{EN}$ | Control inputs digital input capacitance | $V_{CC}$ = 0 V, $V_{SEL}V_{EN}$ = $V_{CC}$ or GND | | 1 | | pF |
| $C_{I/O(OFF)}$ | OFF-state input capacitance | $V_{CC}$ = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch OFF | | 2 | | pF |
| $C_{I/O(ON)}$ | ON-state input capacitance | $V_{CC}$ = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch ON | | 7.5 | | pF |
| $R_{ON}$ | ON-state resistance[5] | $V_{CC}$ = 3 V, $V_I$ = 0.4, $I_O$ = –8 mA | | 6 | 10 | Ω |
| $\Delta R_{ON}$ | ON-state resistance match between channels | $V_{CC}$ = 3 V, $V_I$ = 0.4, $I_O$ = –8 mA | | 0.35 | | Ω |
| $r_{on(flat)}$ | ON-state resistance flatness | $V_{CC}$ = 3 V, $V_I$ = 0 V or 1 V, $I_O$ = –8 mA | | 2 | | Ω |

(1) $V_I$, $V_O$, $I_I$, and $I_O$ refer to data I/O pins A, B, An, and Bn.
(2) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each digital control input that is supplied with a voltage other than $V_{CC}$ or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 6.6 Dynamic Electrical Characteristics

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3 V ± 10%, GND = 0 V

| PARAMETER | | TEST CONDITIONS | TYP(1) | UNIT |
|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, f = 1 MHz, See Figure 6 | –97 | dB |
| $O_{ISO}$ | OFF isolation | $R_L$ = 50 Ω, f = 1 MHz, See Figure 5 | –85 | dB |
| BW | Bandwidth (–3 dB) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 7 | 900 | MHz |

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

## 6.7 Switching Characteristics

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3 V ± 10%, GND = 0 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay(2) (3) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 8 | | 0.25 | | ns |
| $t_{ON}$ | Line enable time, SEL to A, B, An, or Bn | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 4 | | | 30 | ns |
| $t_{OFF}$ | Line disable time, SEL to A, B, An, or Bn | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 4 | | | 25 | ns |
| $t_{ON}$ | Line enable time, $\overline{OE}$ to A, B, An, or Bn | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 4 | | | 30 | ns |
| $t_{OFF}$ | Line disable time, $\overline{OE}$ to A, B, An, or Bn | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 4 | | | 25 | ns |
| $t_{SK(O)}$ | Output skew between center port to any other port(2) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 9 | | | 50 | ps |
| $t_{SK(P)}$ | Skew between opposite transitions of the same output ($t_{PHL}$ – $t_{PLH}$)(2) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 9 | | | 20 | ps |

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

## 6.8 Typical Characteristics

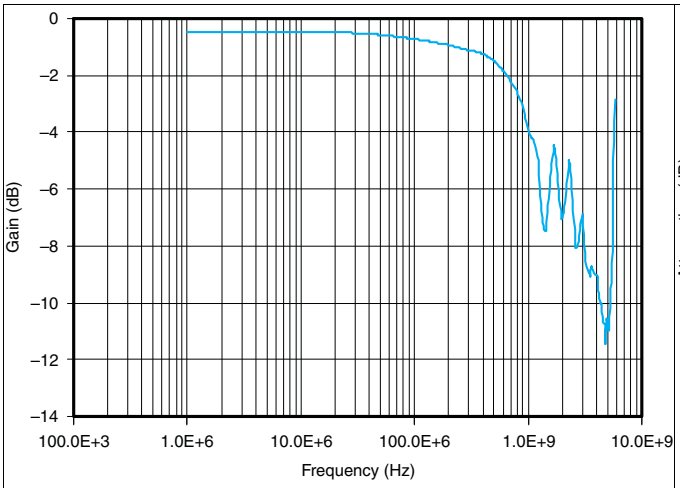



**Figure 1. Bandwidth**

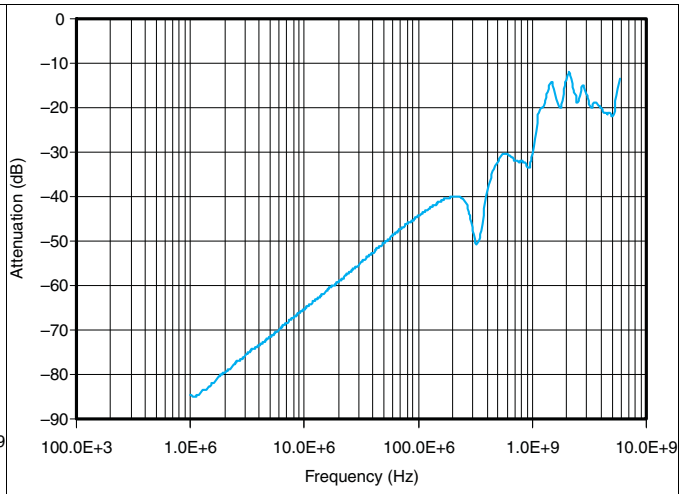



**Figure 2. OFF Isolation**

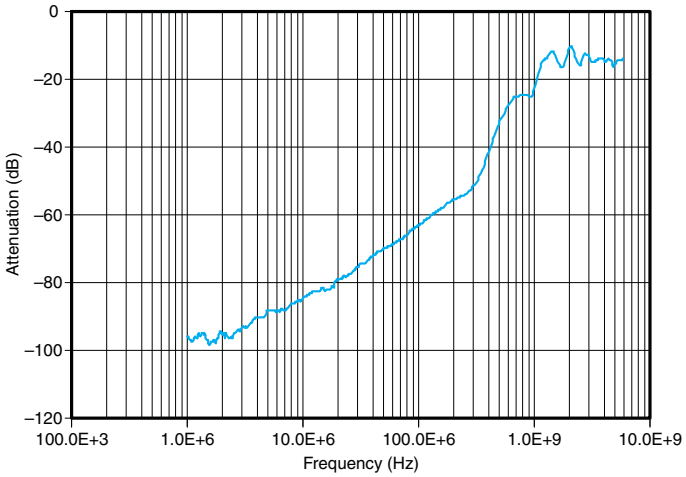
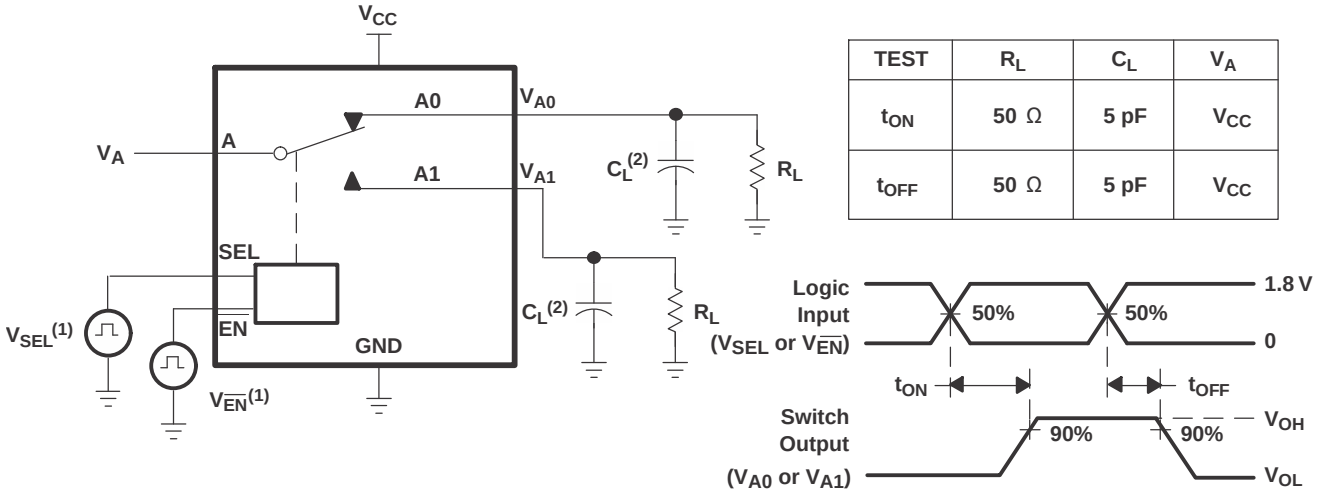



**Figure 3. Crosstalk**

# 7 Parameter Measurement Information



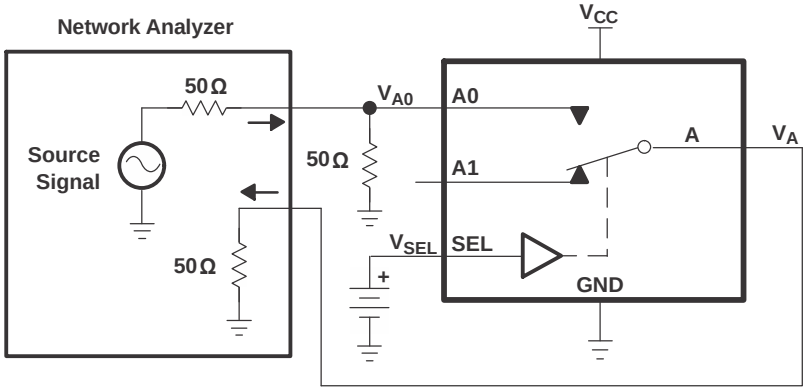

| TEST | $R_L$ | $C_L$ | $V_A$ |
|---|---|---|---|
| $t_{ON}$ | 50 Ω | 5 pF | $V_{CC}$ |
| $t_{OFF}$ | 50 Ω | 5 pF | $V_{CC}$ |



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

(2) $C_L$ includes probe and jig capacitance.

**Figure 4. Turn-On ($t_{ON}$) and Turn-Off Time ($t_{OFF}$)**

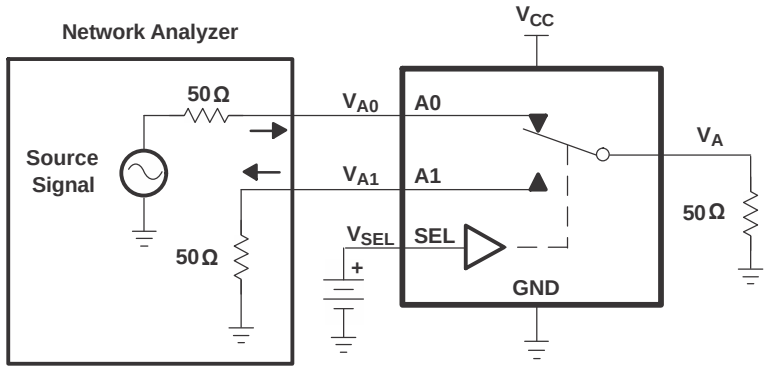



Channel OFF: A to A0
$V_{SEL}$ = $V_{CC}$

Network Analyzer Setup
Source Power = 0 dBm (632-mV P-P at 50-Ω load)
DC Bias = 350 mV



**Figure 5. OFF Isolation ($O_{ISO}$)**




Channel ON: A0 to A
Channel OFF: A1 to A
$V_{SEL}$ = $V_{CC}$

Network Analyzer Setup
Source Power = 0 dBm (632-mV P-P at 50-Ω load)
DC Bias = 350 mV



**Figure 6. Crosstalk ($X_{TALK}$)**

## Parameter Measurement Information (continued)

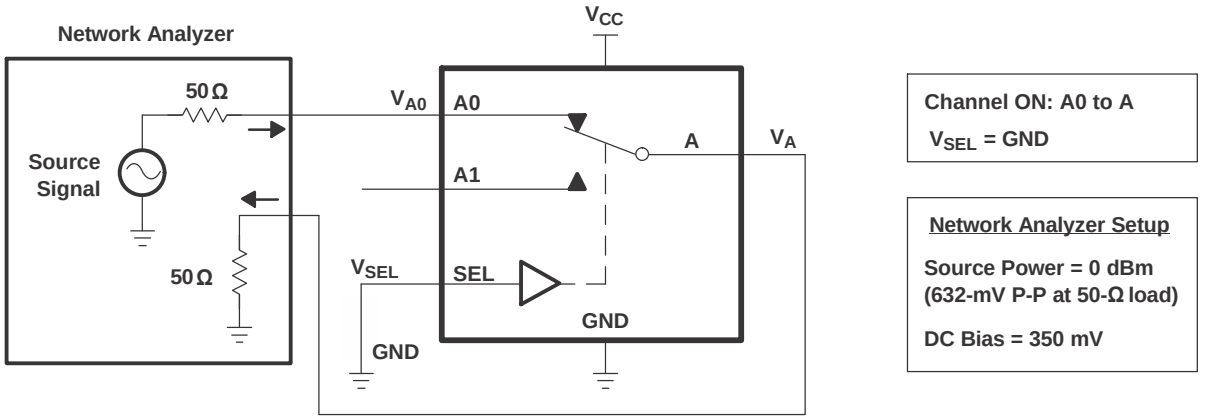





**Figure 7. Bandwidth (BW)**

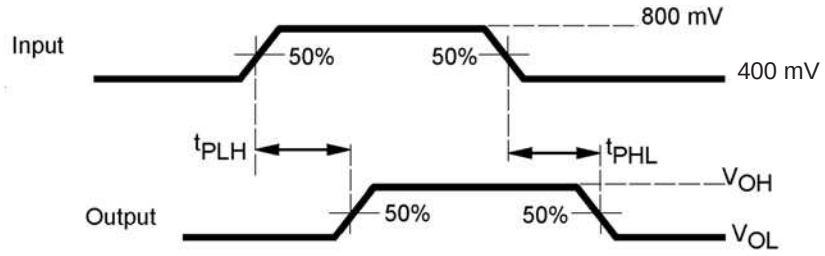
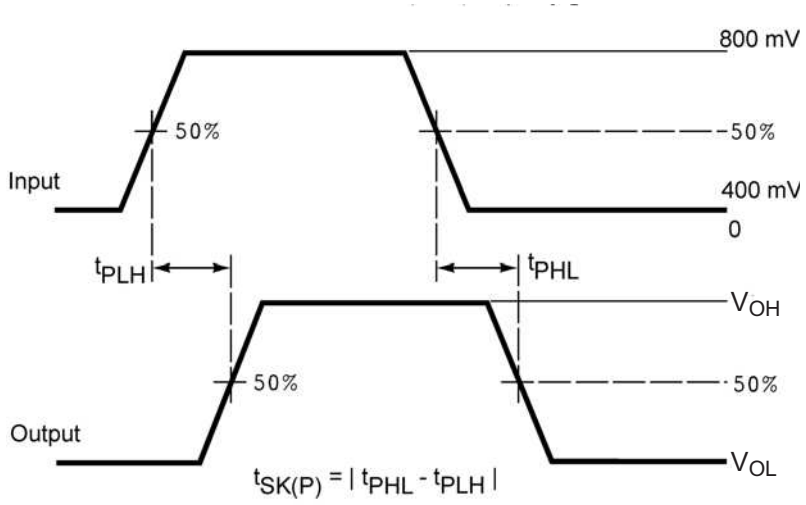
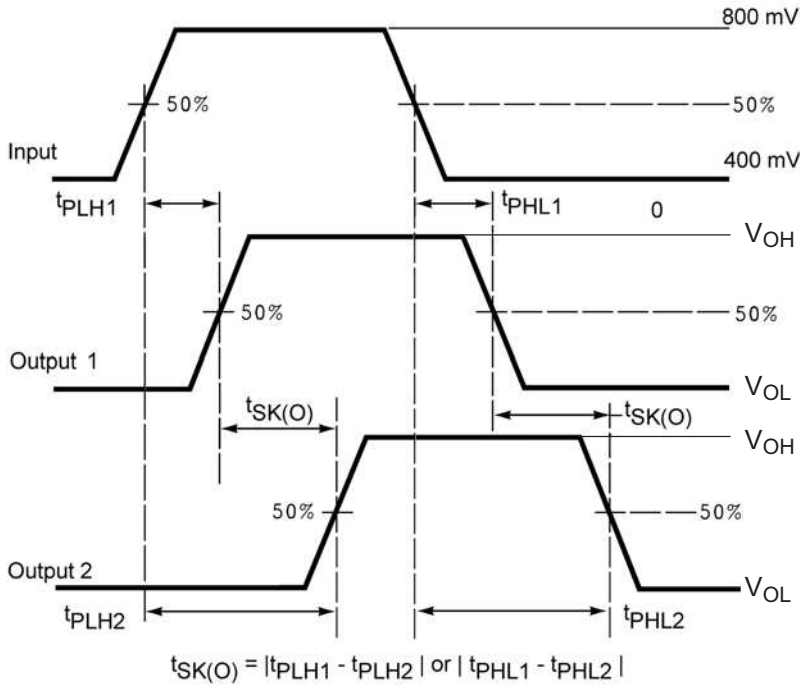



**Figure 8. Propagation Delay**

## Parameter Measurement Information (continued)



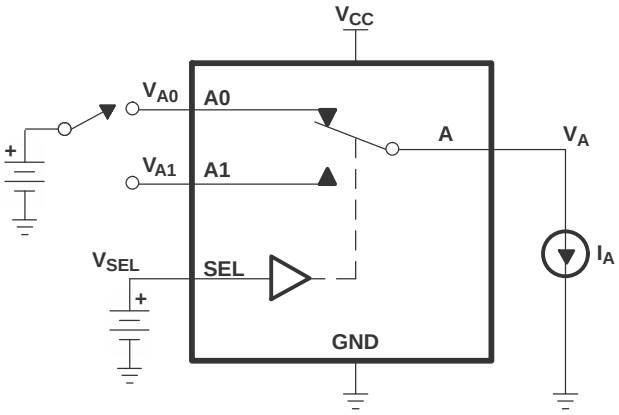

**Pulse Skew $t_{SK(P)}$**




**Output Skew $t_{SK(P)}$**

**Figure 9. Skew Test**

## Parameter Measurement Information (continued)



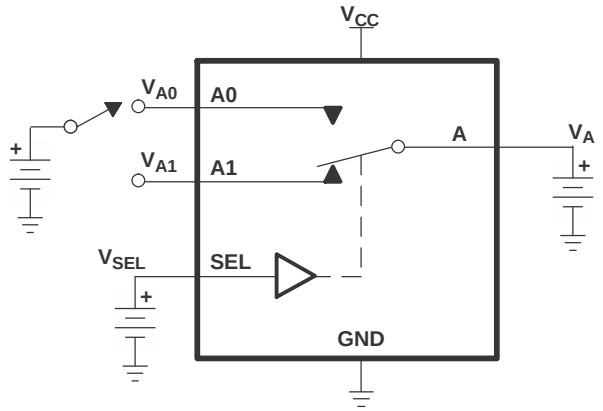

**Channel ON**

$$r_{on} = \frac{V_A - V_{A0}}{I_{IN}}$$

$V_{SEL}$ = GND



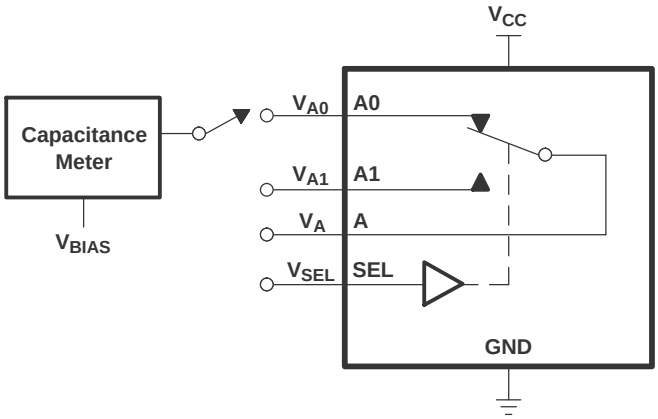
**Figure 10. ON-State Resistance ($R_{ON}$)**




**OFF-State Leakage Current**
**Channel OFF**
$V_{SEL} = V_{IH}$ or $V_{CC}$



**Figure 11. OFF-State Leakage Current**




$V_{BIAS} = V_{CC}$ or GND

$V_{SEL} = V_{CC}$ or GND

**Capacitance is measured at A0, A1, A and SEL inputs during on and off conditions**



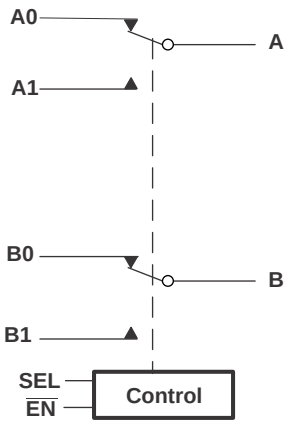
**Figure 12. Capacitance**

# 8 Detailed Description

## 8.1 Overview

The TMUX154E is a high-bandwidth switch specially designed for the switching and isolating of high-speed signals in systems with limited I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential or single ended signals from a single device to one of two corresponding outputs or from two different different devices to one single output. The switch is bidirectional and offers little or no attenuation of the high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

The TMUX154E has an enable pin $\overline{EN}$ that can place the signal paths in high impedance. This allows the user to isolate the signal path when it is not in use and consume less current.

## 8.4 Device Functional Modes

The device functional modes are shown in Table 1.

**Table 1. Truth Table**

| SEL | $\overline{EN}$ | FUNCTION |
|---|---|---|
| X | H | Disconnect |
| L | L | A = A0<br>B= B0 |
| H | L | A = A1<br>B = B1 |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

There are many applications in which processors and microcontrollers have a limited number of I/Os. The TMUX154E solution can effectively expand the limited number of I/Os by switching between multiple signal paths in order to interface them to a single processor or microcontroller. TMUX154E can also be used to connect a single microcontroller to two signal paths.

## 9.2 Typical Application

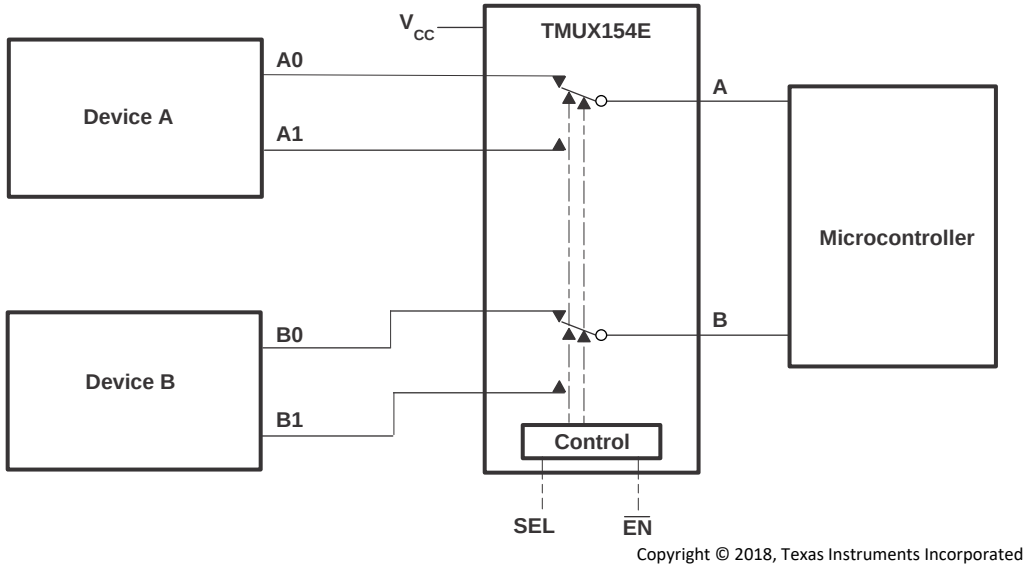




**Figure 13. Application Diagram**

### 9.2.1 Design Requirements

TI recommends that the digital control pins SEL and $\overline{EN}$ be pulled up to $V_{CC}$ or down to GND to avoid undesired switch positions that could result from the floating pin.

### 9.2.2 Detailed Design Procedure

The TMUX154E can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

## Typical Application (continued)

### 9.2.3 Application Curves

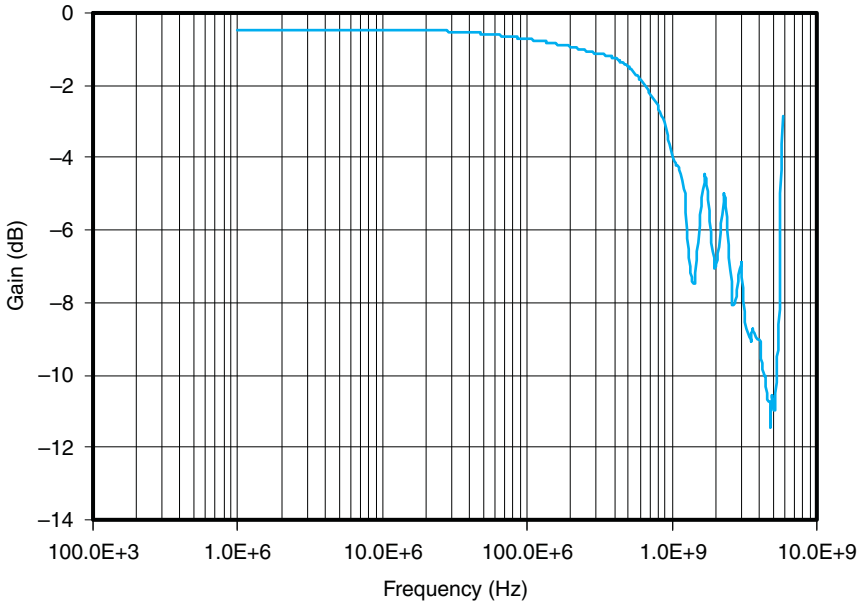



**Figure 14. Bandwidth**

# 10 Power Supply Recommendations

TI recommends placing a bypass capacitor as close as possible to the supply pin $V_{CC}$ to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

# 11 Layout

## 11.1 Layout Guidelines

Place supply bypass capacitors as close to $V_{CC}$ pin as possible and avoid placing the bypass caps near the signal traces.

The high-speed traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded.

Route the high-speed signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed signals because they cause signal reflections.

Route all high-speed signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

For high frequency systems, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082)

## 11.2 Layout Example

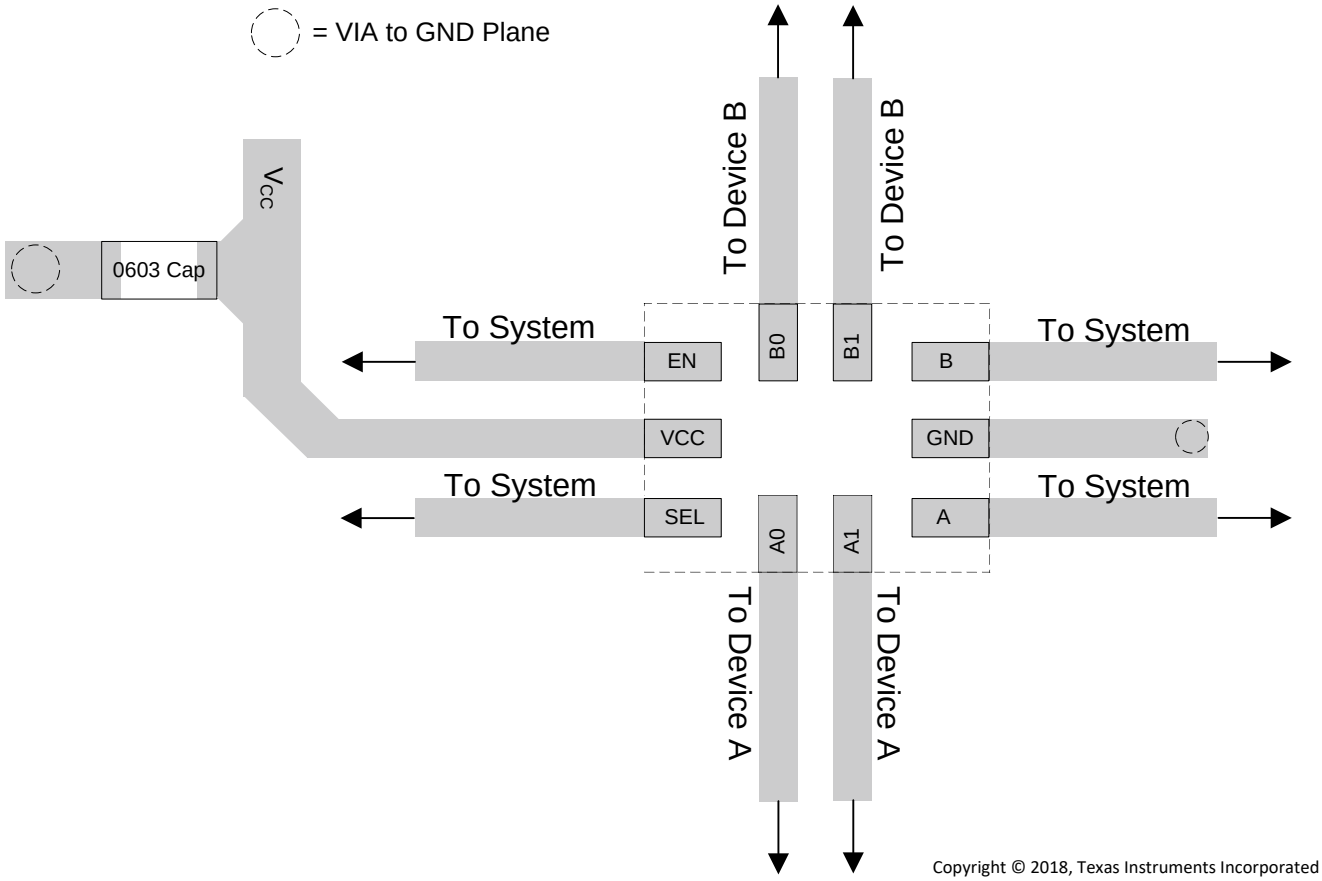



**Figure 15. Layout Recommendation**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *High Speed Layout Guidelines*, SCAA082

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMUX154EDGSR | Active | Production | VSSOP (DGS) \| 10 | 2500 \| LARGE T&R | Yes | NIPDAUAG \| SN | Level-1-260C-UNLIM | -40 to 85 | 1A6 |
| TMUX154EDGSR.B | Active | Production | VSSOP (DGS) \| 10 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | 1A6 |
| TMUX154ERSWR | Active | Production | UQFN (RSW) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BXV |
| TMUX154ERSWR.B | Active | Production | UQFN (RSW) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BXV |
| TMUX154ERSWRG4 | Active | Production | UQFN (RSW) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BXV |
| TMUX154ERSWRG4.B | Active | Production | UQFN (RSW) \| 10 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BXV |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

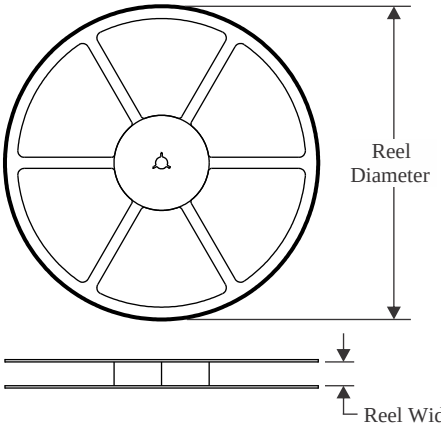
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# PACKAGE MATERIALS INFORMATION

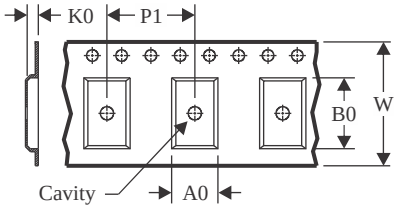
18-Jun-2025

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

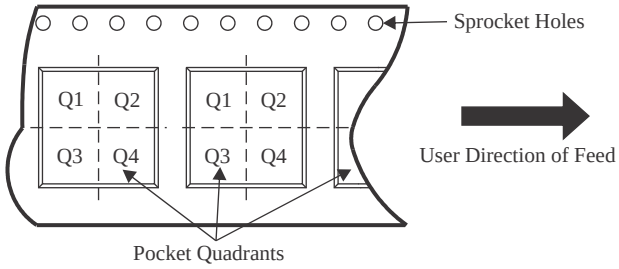



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



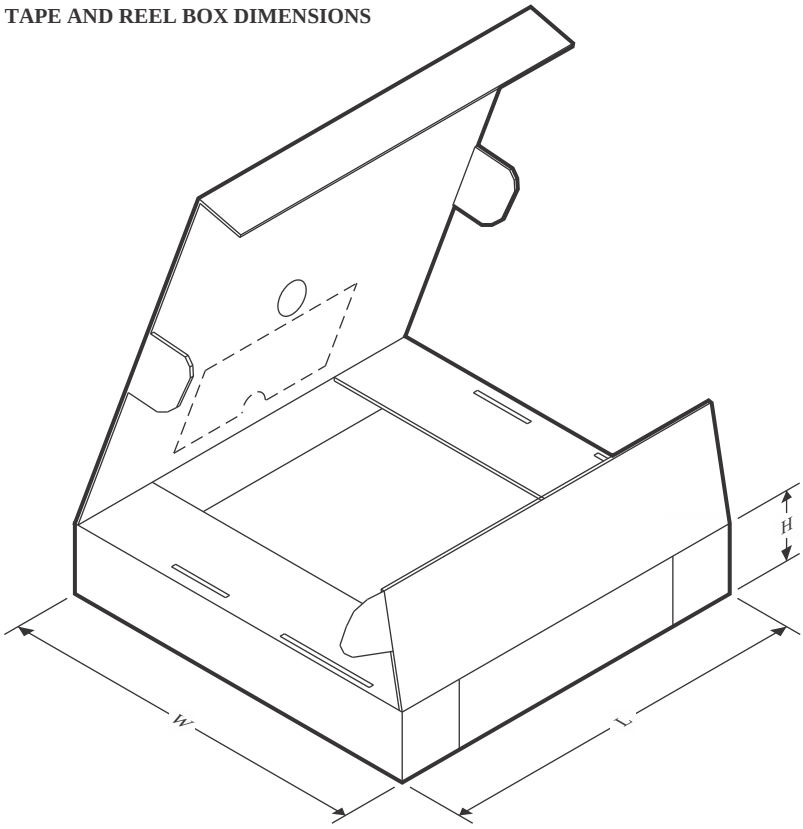

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX154EDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.25 | 3.35 | 1.25 | 8.0 | 12.0 | Q1 |
| TMUX154ERSWR | UQFN | RSW | 10 | 3000 | 180.0 | 9.5 | 1.6 | 2.0 | 0.8 | 4.0 | 8.0 | Q1 |
| TMUX154ERSWR | UQFN | RSW | 10 | 3000 | 180.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| TMUX154ERSWRG4 | UQFN | RSW | 10 | 3000 | 180.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

18-Jun-2025

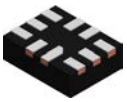
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX154EDGSR | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |
| TMUX154ERSWR | UQFN | RSW | 10 | 3000 | 189.0 | 185.0 | 36.0 |
| TMUX154ERSWR | UQFN | RSW | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TMUX154ERSWRG4 | UQFN | RSW | 10 | 3000 | 210.0 | 185.0 | 35.0 |

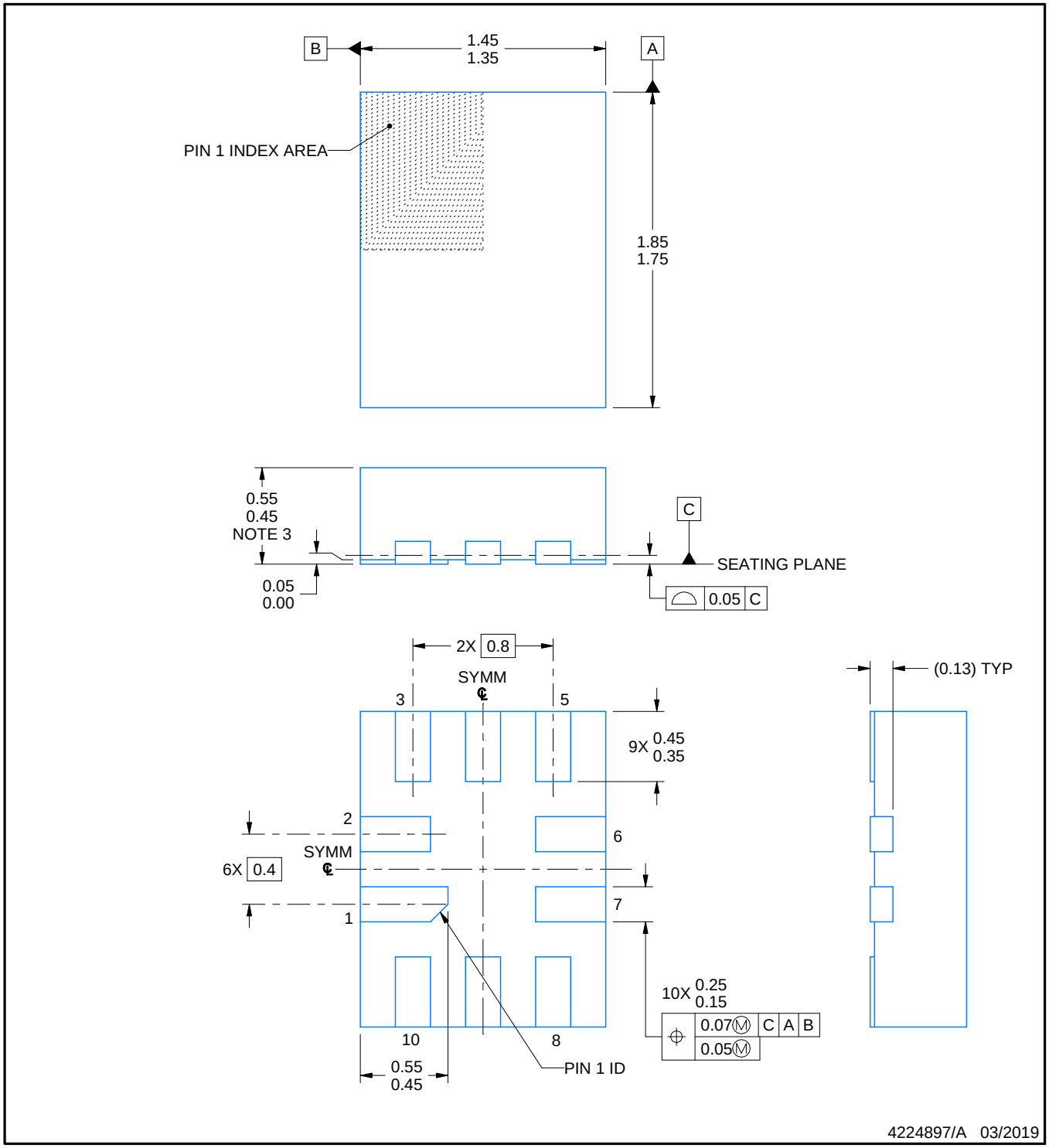
# RSW0010A



# PACKAGE OUTLINE

## UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

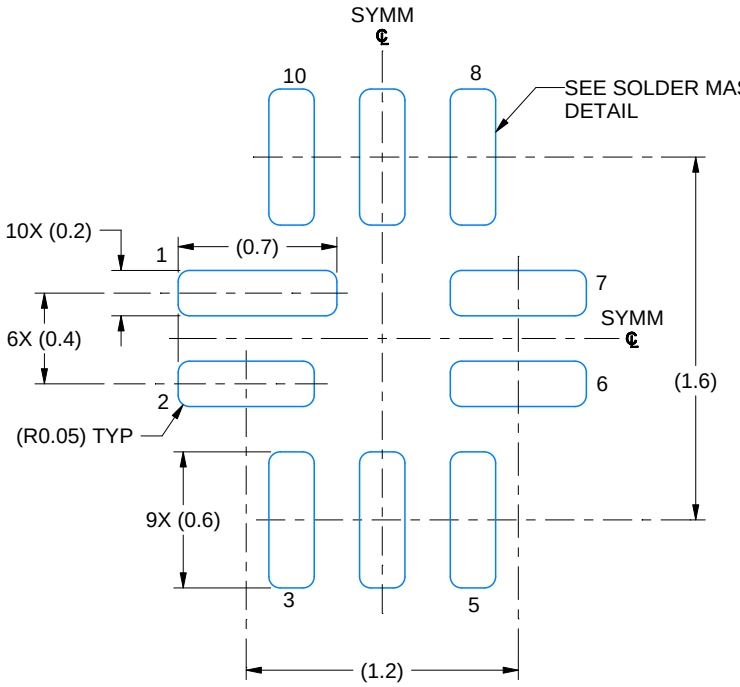
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

# EXAMPLE BOARD LAYOUT

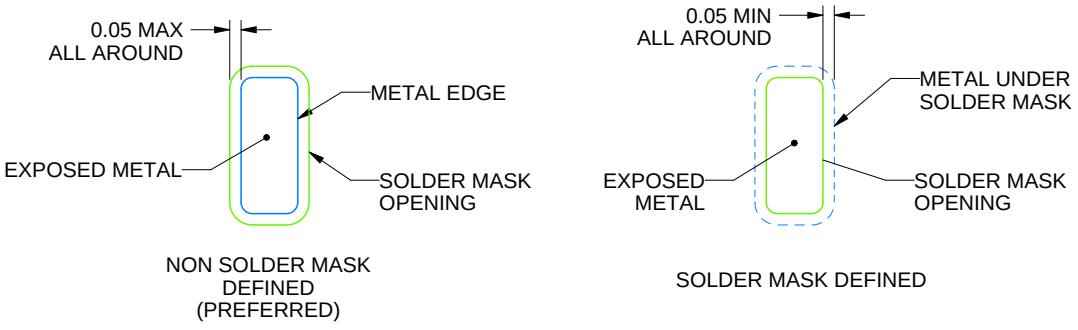
## RSW0010A

## UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X




SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

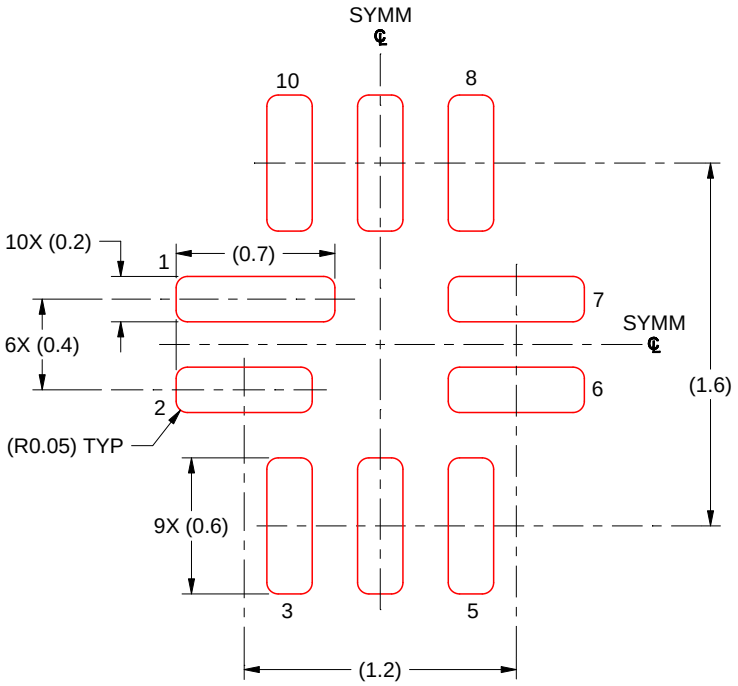
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## RSW0010A

## UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

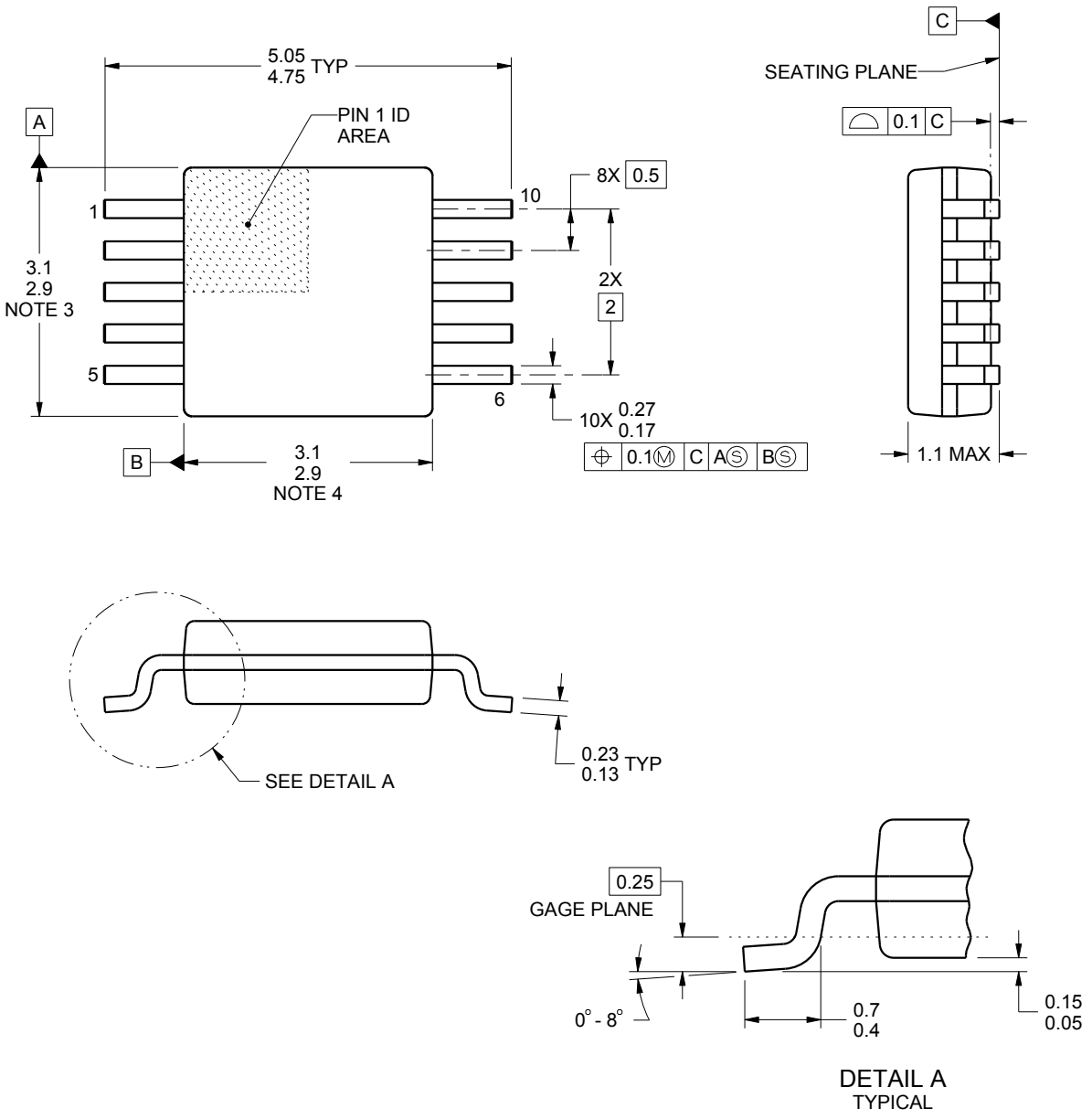
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DGS0010A

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




4221984/A 05/2015

NOTES:

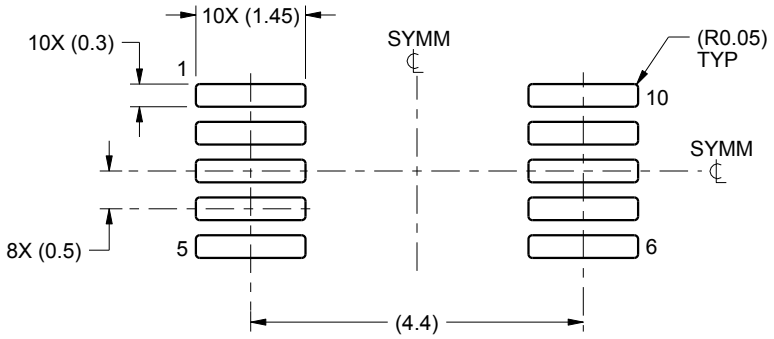
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

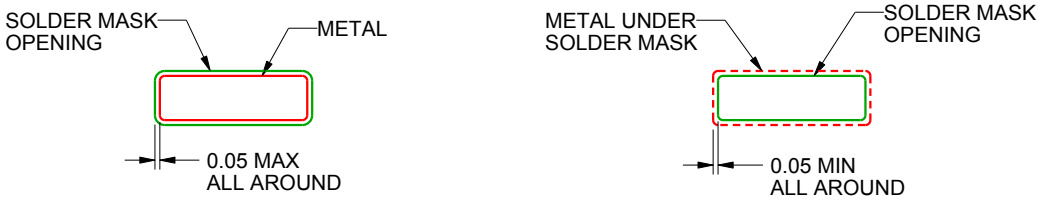
## DGS0010A

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

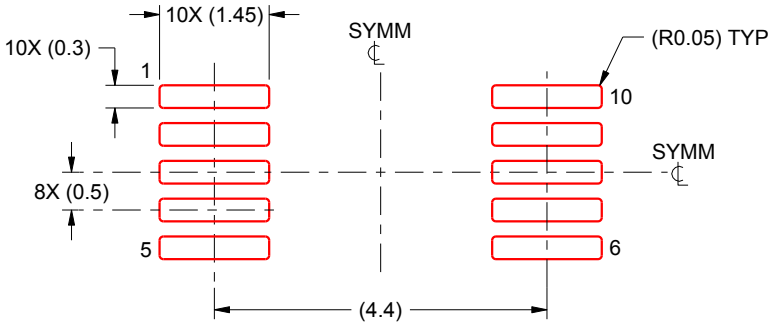
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DGS0010A

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.