MUX50x
36-V, Low-Capacitance, Low-Charge-Injection, Precision, Analog Multiplexers

1 Features

- Low On-Capacitance
  - MUX508: 9.4 pF
  - MUX509: 6.7 pF
- Low Input Leakage: 10 pA
- Low Charge Injection: 0.3 pC
- Rail-to-Rail Operation
- Wide Supply Range: ±5 V to ±18 V, 10 V to 36 V
- Low On-Resistance: 125 Ω
- Transition Time: 92 ns
- Break-Before-Make Switching Action
- EN Pin Connectable to V_{DD}
- Logic Levels: 2 V to V_{DD}
- Low Supply Current: 45 µA
- ESD Protection HBM: 2000 V
- Industry-Standard TSSOP and SOIC Packages

2 Applications

- Factory Automation and Industrial Process Controls
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- ATE Test Equipment
- Digital Multimeters
- Battery Monitoring Systems

3 Description

The MUX508 and MUX509 (MUX50x) are modern, complementary metal-oxide semiconductor (CMOS), analog multiplexers (muxes). The MUX508 offers 8:1 single-ended channels, whereas the MUX509 offers differential 4:1 or dual 4:1 single-ended channels. The MUX508 and MUX509 work equally well with either dual supplies (±5 V to ±18 V) or a single supply (10 V to 36 V). They also perform well with symmetric supplies (such as V_{DD} = 12 V, V_{SS} = –12 V), and unsymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). All digital inputs have TTL-logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

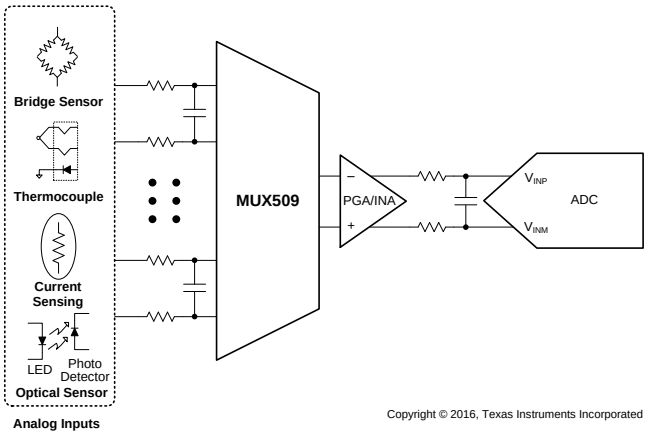
The MUX508 and MUX509 have very low on and off leakage currents, allowing these multiplexers to switch signals from high input impedance sources with minimal error. A low supply current of 45 µA allows for use in portable applications.

Device Information(1)

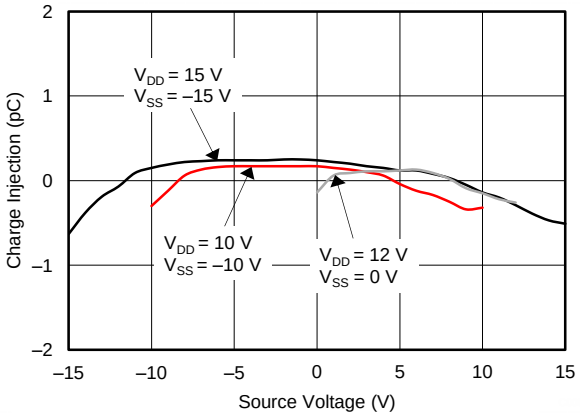
PART NUMBER	PACKAGE	BODY SIZE (NOM)
MUX50x	TSSOP (16)	5.00 mm × 4.40 mm
	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



Charge Injection vs Source Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2016) to Revision C **Page**

- Added D (SOIC) package to document ... 1
- Changed last Features bullet to include SOIC package ... 1
- Changed second sentence of *Description* section ... 1
- Added SOIC package to *Device Information* table ... 1
- Changed MUX509 description in *Device Comparison Table* ... 4
- Added D package to *Pin Configuration and Functions* section ... 4
- Added D package to *Thermal Information* table ... 7
- Changed Analog Switch, I_D parameter in *Electrical Characteristics: Dual Supply* table: split parameter into $I_{D(OFF)}$ and $I_{D(ON)}$ parameters, changed symbols, parameter names, and test conditions ... 7
- Changed *On-resistance drift* parameter in *Electrical Characteristics: Single Supply* table: changed V_S value in test conditions ... 9
- Changed Analog Switch, I_D parameter in *Electrical Characteristics: Single Supply* table: split parameter into $I_{D(OFF)}$ and $I_{D(ON)}$ parameters, changed symbols, parameter names, and $I_{D(ON)}$ test conditions ... 9
- Changed Figure 26: changed switch symbol to a closed switch symbol ... 16
- Changed Figure 32: added 0 V line, flipped V_S supply symbol ... 20
- Changed description of MUX509 in *Overview* section ... 23
- Changed Figure 42: changed OPA140 amplifier and charge kickback filter box ... 27
- Added D package description to *Layout Guidelines* section ... 30

Changes from Revision A (March 2016) to Revision B **Page**

- Added TI Design 1
- Changed Analog Switch, $I_{S(OFF)}$ and I_D parameter specifications in *Electrical Characteristics: Single Supply* table..... 9

Changes from Original (January 2016) to Revision A **Page**

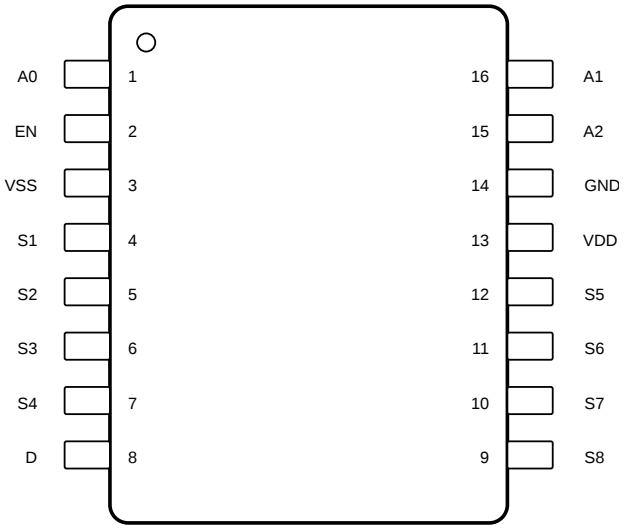
- Changed from product preview to production data 1

5 Device Comparison Table

PRODUCT	DESCRIPTION
MUX508	8-channel, single-ended analog multiplexer (8:1 mux)
MUX509	4-channel differential or dual 4:1 single-ended analog multiplexer (8:2 mux)

6 Pin Configuration and Functions

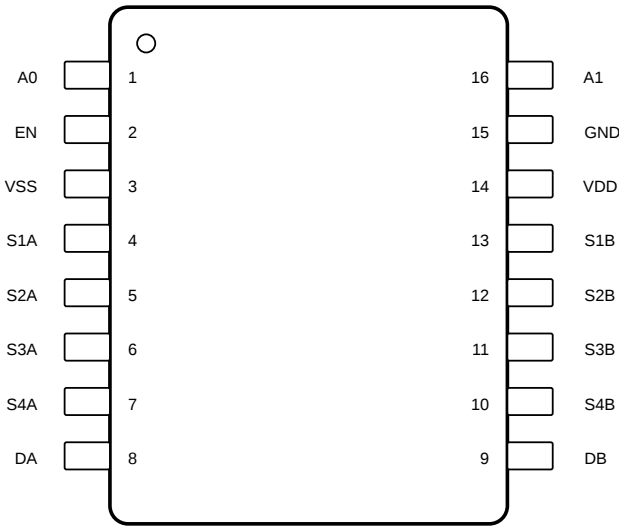
MUX508: PW and D Packages
16-Pin TSSOP and SOIC
Top View



Pin Functions: MUX508

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Digital input	Address line 0
A1	16	Digital input	Address line 1
A2	15	Digital input	Address line 2
D	8	Analog input or output	Drain pin. Can be an input or output.
EN	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which switch is turned on.
GND	14	Power supply	Ground (0 V) reference
S1	4	Analog input or output	Source pin 1. Can be an input or output.
S2	5	Analog input or output	Source pin 2. Can be an input or output.
S3	6	Analog input or output	Source pin 3. Can be an input or output.
S4	7	Analog input or output	Source pin 4. Can be an input or output.
S5	12	Analog input or output	Source pin 5. Can be an input or output.
S6	11	Analog input or output	Source pin 6. Can be an input or output.
S7	10	Analog input or output	Source pin 7. Can be an input or output.
S8	9	Analog input or output	Source pin 8. Can be an input or output.
VDD	13	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	3	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND.

MUX509: PW and D Packages
16-Pin TSSOP and SOIC
Top View



Pin Functions: MUX509

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	1	Digital input	Address line 0
A1	16	Digital input	Address line 1
DA	8	Analog input or output	Drain pin A. Can be an input or output.
DB	9	Analog input or output	Drain pin B. Can be an input or output.
EN	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which pair of switches is turned on.
GND	15	Power supply	Ground (0 V) reference
S1A	4	Analog input or output	Source pin 1A. Can be an input or output.
S2A	5	Analog input or output	Source pin 2A. Can be an input or output.
S3A	6	Analog input or output	Source pin 3A. Can be an input or output.
S4A	7	Analog input or output	Source pin 4A. Can be an input or output.
S1B	13	Analog input or output	Source pin 1B. Can be an input or output.
S2B	12	Analog input or output	Source pin 2B. Can be an input or output.
S3B	11	Analog input or output	Source pin 3B. Can be an input or output.
S4B	10	Analog input or output	Source pin 4B. Can be an input or output.
VDD	14	Power supply	Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	3	Power supply	Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_{DD}		–0.3	40	V
	V_{SS}		–40	0.3	
	$V_{DD} – V_{SS}$			40	
Digital input pins(2)	EN, A0, A1, A2 pins	Voltage	$V_{SS} – 0.3$	$V_{DD} + 0.3$	V
		Current	–30	30	mA
Analog input pins(2)	Sx, SxA, SxB pins	Voltage	$V_{SS} – 2$	$V_{DD} + 2$	V
		Current	–30	30	mA
Analog output pins(2)	D, DA, DB pins	Voltage	$V_{SS} – 2$	$V_{DD} + 2$	V
		Current	–30	30	mA
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Only one pin at a time

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}(1)	Positive power-supply voltage	Dual supply	5		18	V
		Single supply	10		36	
V_{SS}(2)	Negative power-supply voltage (dual supply)		–5		–18	V
$V_{DD} – V_{SS}$	Supply voltage		10		36	V
V_S	Source pins voltage(3)		V_{SS}		V_{DD}	V
V_D	Drain pins voltage		V_{SS}		V_{DD}	V
V_{EN}	Enable pin voltage		V_{SS}		V_{DD}	V
V_A	Address pins voltage		V_{SS}		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)		–25		25	mA
T_A	Operating temperature		–40		125	°C

(1) When V_{SS} = 0 V, V_{DD} can range from 10 V to 36 V.
(2) V_{DD} and V_{SS} can be any value as long as 10 V ≤ ($V_{DD} – V_{SS}$) ≤ 36 V, and V_{DD} ≥ 5 V.
(3) V_S is the voltage on all the S pins.

7.4 Thermal Information

THERMAL METRIC[1]		MUX50x		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.8	78.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.8	35.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	35.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_{CH} = 1 mA			125	170	Ω
		V_S = ±10 V, I_{CH} = 1 mA			145	200	
			T_A = –40°C to +85°C			230	
			T_A = –40°C to +125°C			250	
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_{CH} = 1 mA			2.4	6	Ω
			T_A = –40°C to +85°C			9	
			T_A = –40°C to +125°C			11	
R_{FLAT}	On-resistance flatness	V_S = 10 V, 0 V, –10 V			22	45	Ω
			T_A = –40°C to +85°C			53	
			T_A = –40°C to +125°C			58	
	On-resistance drift	V_S = 0 V			0.52		%/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V[1]		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–25		25	
$I_{D(OFF)}$	Output off leakage current	Switch state is off, V_S = ±10 V, V_D = ±10 V[1]		–1	0.01	1	nA
			T_A = -40°C to +85°C	–10		10	
			T_A = -40°C to +125°C	–50		50	
$I_{D(ON)}$	Output on leakage current	Switch state is on, V_D = ±10 V, V_S = floating		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–50		50	
LOGIC INPUT							
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
I_D	Input current					0.15	µA

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics: Dual Supply (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SWITCH DYNAMICS(2)							
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF			88	136	ns
			T_A = –40°C to +85°C			144	
			T_A = –40°C to +125°C			151	
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω, C_L= 35 pF			63	75	ns
			T_A = –40°C to +85°C			83	
			T_A = –40°C to +125°C			90	
t_t	Transition time	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF,			92	143	ns
			T_A = –40°C to +85°C			151	
			T_A = –40°C to +125°C			157	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C		30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 0 V		0.3		pC
			V_S = –15 V to +15 V		±0.6		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB		–96		dB
			Adjacent channel to D, DA, DB		–85		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels		–96		dB
			Adjacent channels		–88		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V			2.4	2.9	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	MUX508		7.5	8.4	pF
			MUX509		4.3	5	
$C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	MUX508		9.4	10.6	pF
			MUX509		6.7	7.7	
POWER SUPPLY							
	V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V,			45	59	µA
			T_A = –40°C to +85°C			62	
			T_A = –40°C to +125°C			83	
	V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V,			25	34	µA
			T_A = –40°C to +85°C			37	
			T_A = –40°C to +125°C			57	

(2) Specified by design, not production tested.

7.6 Electrical Characteristics: Single Supply

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_{CH} = 1 mA			235	340	Ω
			T_A = –40°C to +85°C			390	
			T_A = –40°C to +125°C			430	
ΔR_{ON}	On-resistance match	V_S = 10 V, I_{CH} = 1 mA			3.1	12	Ω
			T_A = –40°C to +85°C			19	
			T_A = –40°C to +125°C			23	
	On-resistance drift	V_S = 10 V			0.47		%/°C
$I_{S(OFF)}$	Input leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(2)		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–25		25	
$I_{D(OFF)}$	Output off leakage current	Switch state is off, V_S = 1 V and V_D = 10 V, or V_S = 10 V and V_D = 1 V(2)		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–50		50	
$I_{D(ON)}$	Output on leakage current	Switch state is on, V_D = 1 V and 10 V, V_S = floating		–1	0.01	1	nA
			T_A = –40°C to +85°C	–10		10	
			T_A = –40°C to +125°C	–50		50	
LOGIC INPUT							
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
I_D	Input current					0.15	µA
SWITCH DYNAMIC CHARACTERISTICS							
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF			85	140	ns
			T_A = –40°C to +85°C			145	
			T_A = –40°C to +125°C			149	
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF			48	83	ns
			T_A = –40°C to +85°C			94	
			T_A = –40°C to +125°C			102	
t_t	Transition time	V_S = 8 V, C_L= 35 pF			87	147	ns
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF,	T_A = –40°C to +85°C			153	
		V_S = 8 V, R_L = 300 Ω, C_L= 35 pF,	T_A = –40°C to +125°C			155	
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L= 35 pF, T_A = –40°C to +125°C		30	54		ns
Q_J	Charge injection	C_L = 1 nF, R_S = 0 Ω	V_S = 6 V		0.15		pC
			V_S = 0 V to 12 V,		±0.4		
	Off-isolation	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channel to D, DA, DB		-96		dB
			Adjacent channel to D, DA, DB		-85		
	Channel-to-channel crosstalk	R_L = 50 Ω, V_S = 1 V_{RMS}, f = 1 MHz	Nonadjacent channels		–96		dB
			Adjacent channels		-88		
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V			2.7	3.2	pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	MUX508		9.1	10	pF
			MUX509		5	5.7	
$C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 6 V	MUX508		10.8	12	pF
			MUX509		6.9	8	

(1) Specified by design, not production tested.
(2) When V_S is 1 V, V_D is 10 V, and vice versa.

Electrical Characteristics: Single Supply (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)[1]

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD} supply current	All V_A = 0 V or 3.3 V, V_S= 0 V, V_{EN} = 3.3 V			42	53	µA
		T_A = –40°C to +85°C			56	
		T_A = –40°C to +125°C			77	
V_{SS} supply current	All V_A = 0 V or 3.3 V, V_S = 0 V, V_{EN} = 3.3 V			23	38	µA
		T_A = –40°C to +85°C			31	
		T_A = –40°C to +125°C			51	

7.7 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

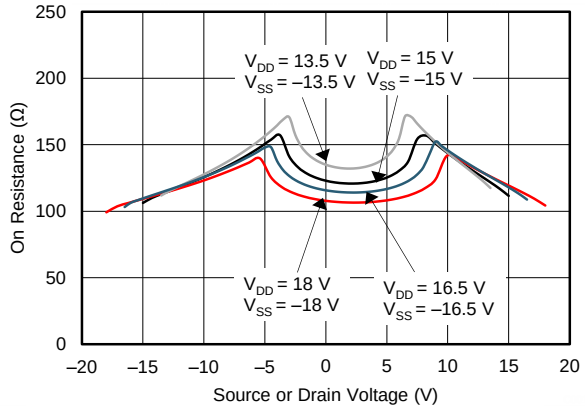
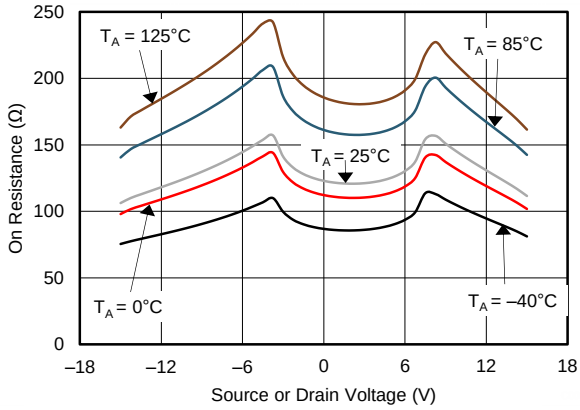


Figure 1. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

Figure 2. On-Resistance vs Source or Drain Voltage

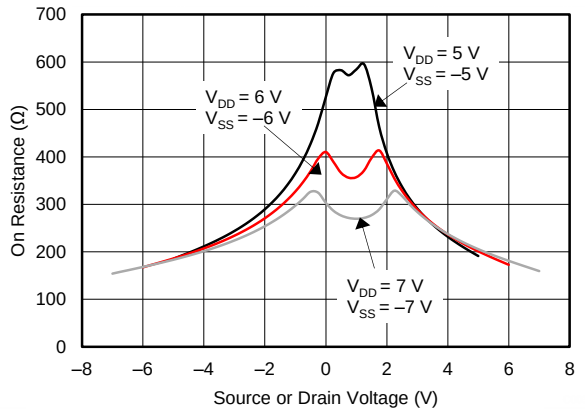
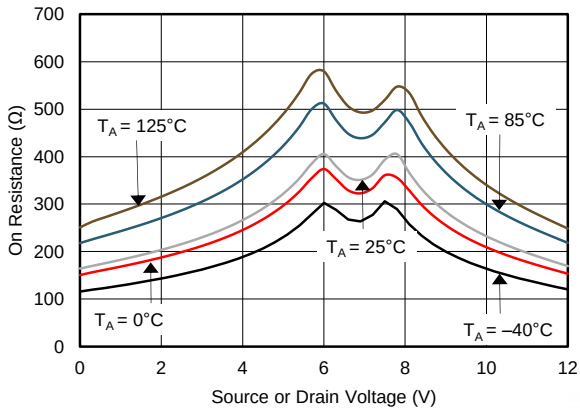


Figure 3. On-Resistance vs Source or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 4. On-Resistance vs Source or Drain Voltage

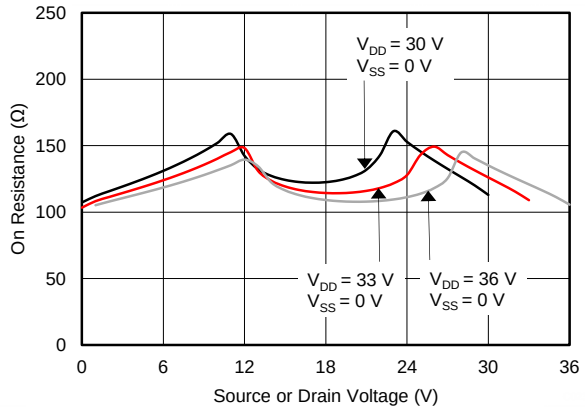


Figure 5. On-Resistance vs Source or Drain Voltage

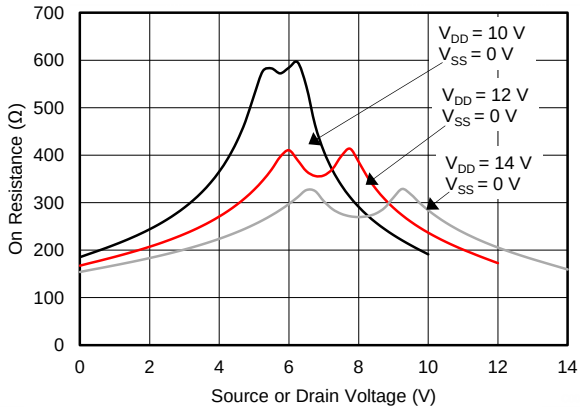
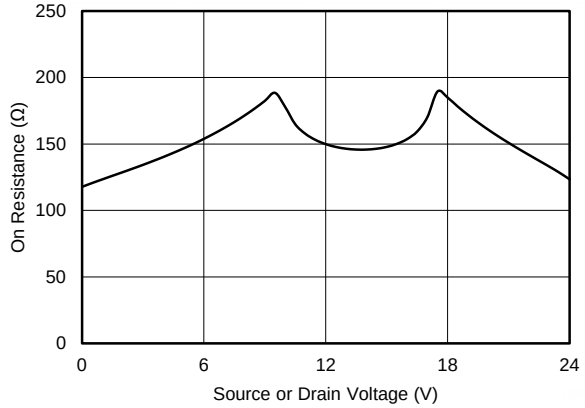


Figure 6. On-Resistance vs Source or Drain Voltage

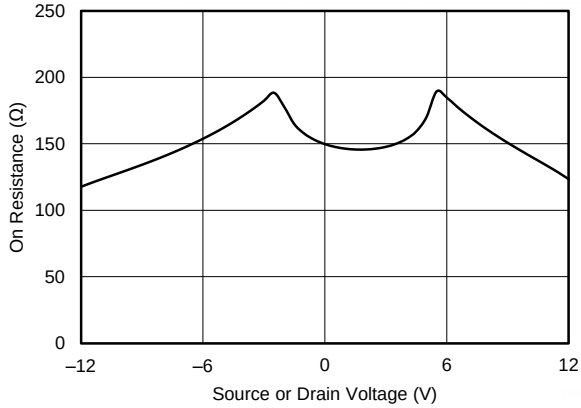
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



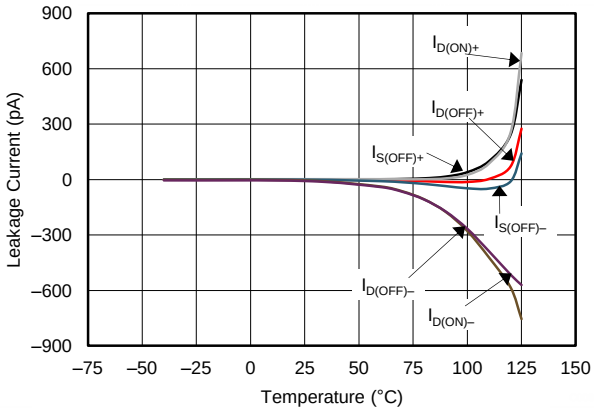
V_{DD} = 24 V, V_{SS} = 0 V

Figure 7. On-Resistance vs Source or Drain Voltage



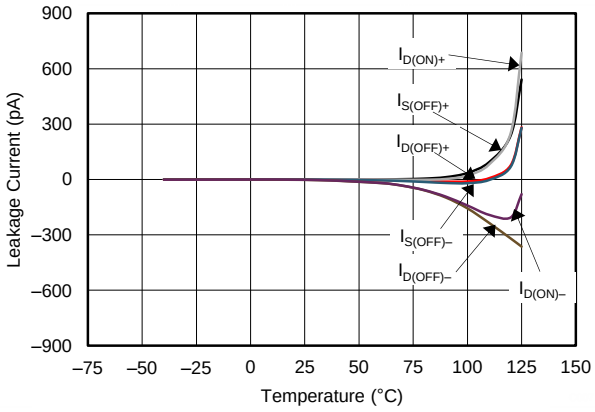
V_{DD} = 12 V, V_{SS} = –12 V

Figure 8. On-Resistance vs Source or Drain Voltage



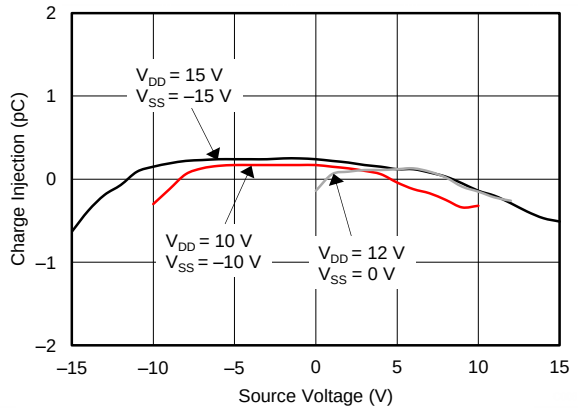
V_{DD} = 15 V, V_{SS} = –15 V

Figure 9. Leakage Current vs Temperature



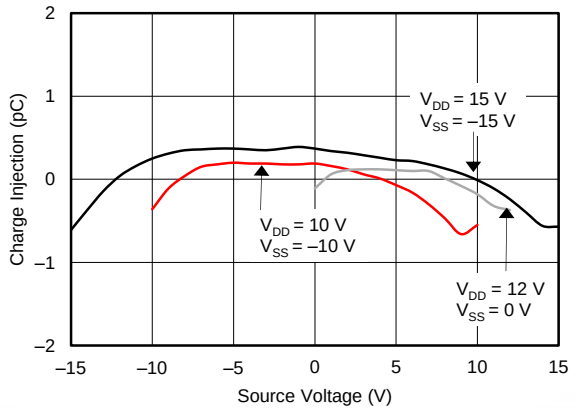
V_{DD} = 12 V, V_{SS} = 0 V

Figure 10. Leakage Current vs Temperature



MUX508, source-to-drain

Figure 11. Charge Injection vs Source Voltage



MUX509, source-to-drain

Figure 12. Charge Injection vs Source Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

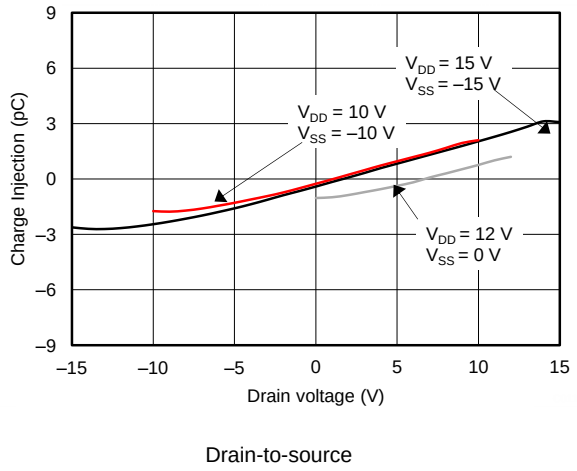


Figure 13. Charge Injection vs Source or Drain Voltage

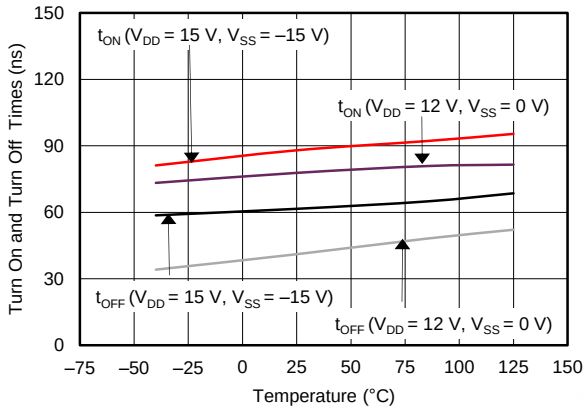


Figure 14. Turn-On and Turn-Off Times vs Temperature

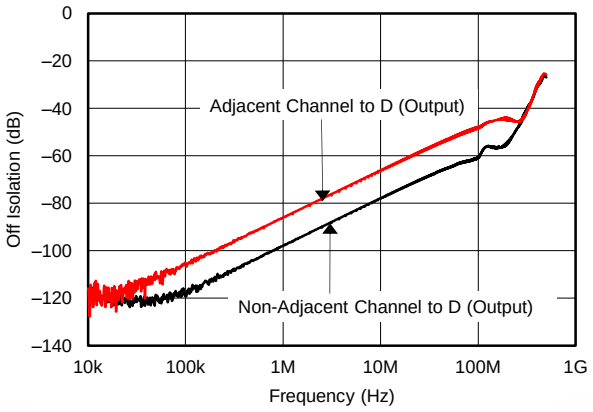


Figure 15. Off Isolation vs Frequency

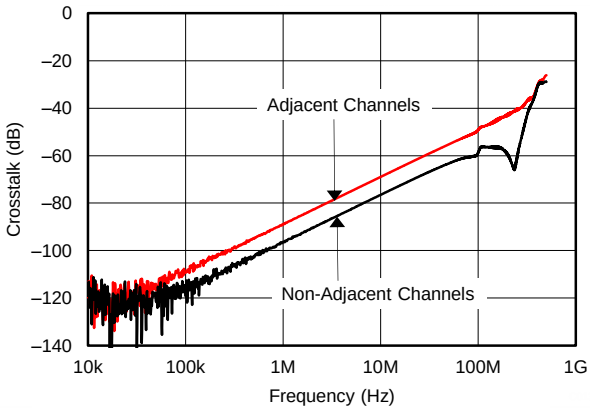


Figure 16. Crosstalk vs Frequency

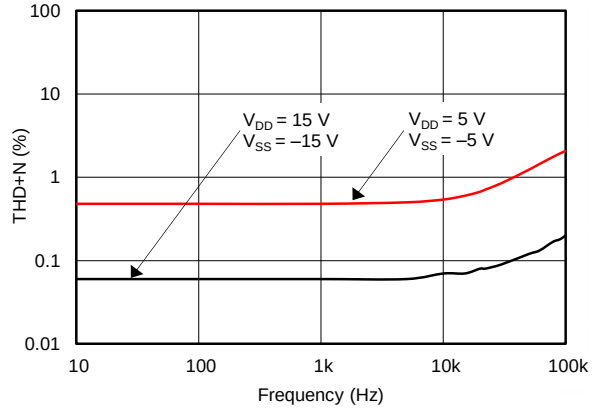


Figure 17. THD+N vs Frequency

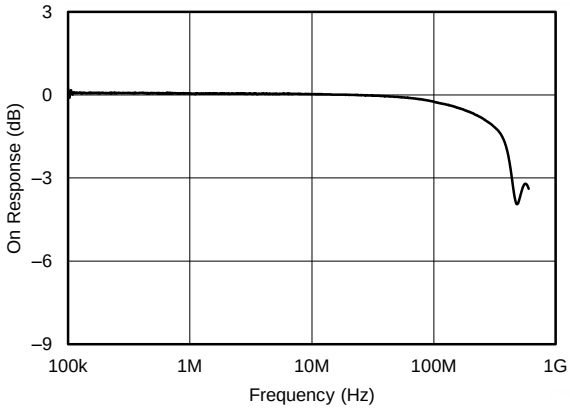
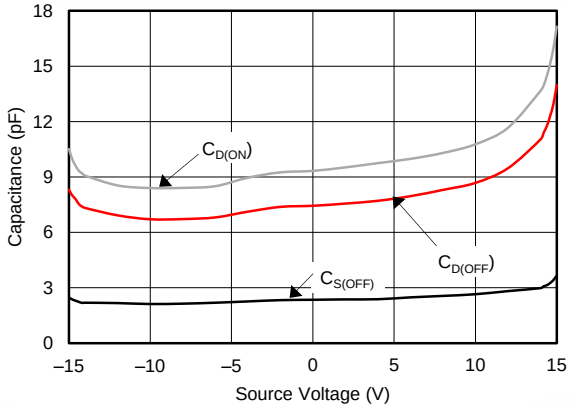


Figure 18. On Response vs Frequency

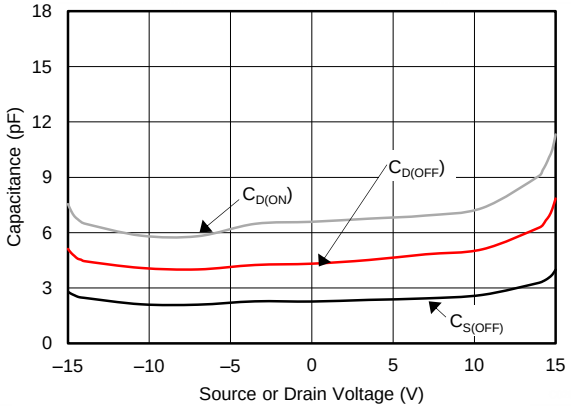
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



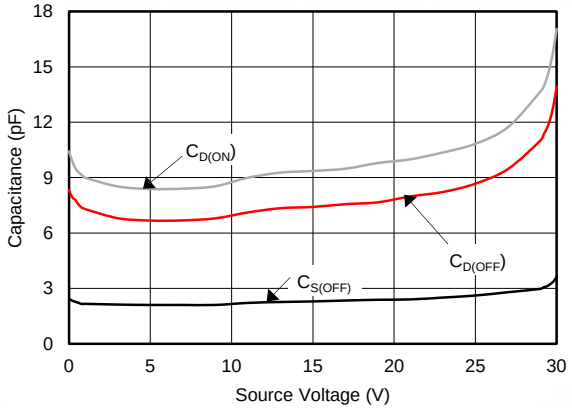
MUX508, V_{DD} = 15 V, V_{SS} = –15 V

Figure 19. Capacitance vs Source Voltage



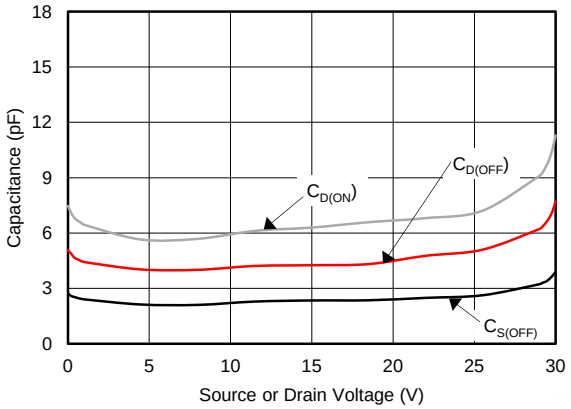
MUX509, V_{DD} = 15 V, V_{SS} = –15 V

Figure 20. Capacitance vs Source Voltage



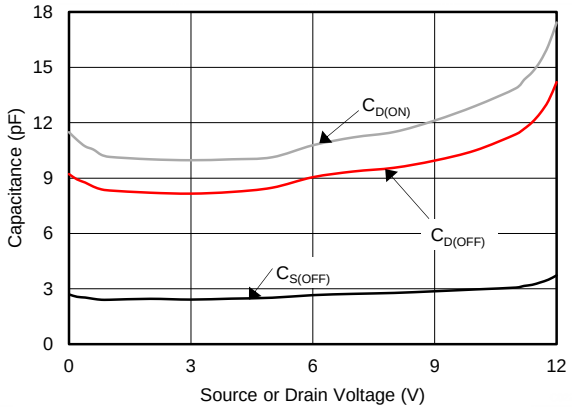
MUX508, V_{DD} = 30 V, V_{SS} = 0 V

Figure 21. Capacitance vs Source Voltage



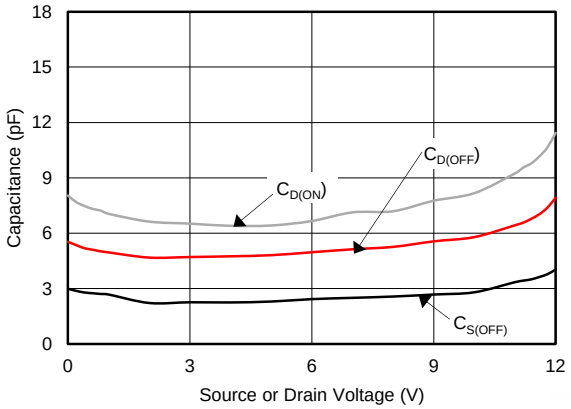
MUX509, V_{DD} = 30 V, V_{SS} = 0 V

Figure 22. Capacitance vs Source Voltage



MUX508, V_{DD} = 12 V, V_{SS} = 0 V

Figure 23. Capacitance vs Source Voltage



MUX509, V_{DD} = 12 V, V_{SS} = 0 V

Figure 24. Capacitance vs Source Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

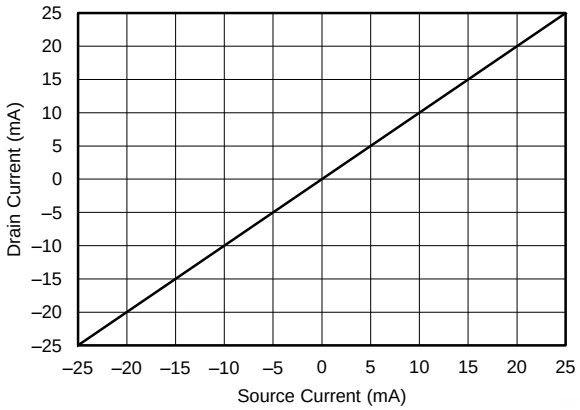


Figure 25. Source Current vs Drain Current

8 Parameter Measurement Information

8.1 Truth Tables

Table 1 and Table 2 show the truth tables for the MUX508 and MUX509, respectively.

Table 1. MUX508 Truth Table

EN	A2	A1	A0	STATE
0	X(1)	X(1)	X(1)	All channels are off
1	0	0	0	Channel 1 on
1	0	0	1	Channel 2 on
1	0	1	0	Channel 3 on
1	0	1	1	Channel 4 on
1	1	0	0	Channel 5 on
1	1	0	1	Channel 6 on
1	1	1	0	Channel 7 on
1	1	1	1	Channel 8 on

(1) X denotes *don't care*..

Table 2. MUX509 Truth Table

EN	A1	A0	STATE
0	X(1)	X(1)	All channels are off
1	0	0	Channels 1A and 1B on
1	0	1	Channels 2A and 2B on
1	1	0	Channels 3A and 3B on
1	1	1	Channels 4A and 4B on

(1) X denotes *don't care*.

8.2 On-Resistance

The on-resistance of the MUX50x is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 26. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1.

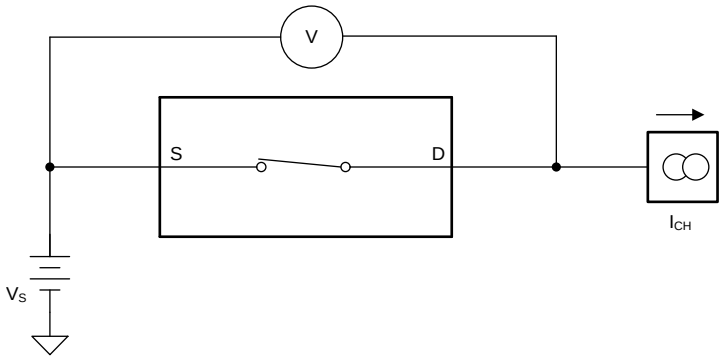


Figure 26. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

8.3 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source off-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain off-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both types of off-leakage currents is shown in Figure 27.

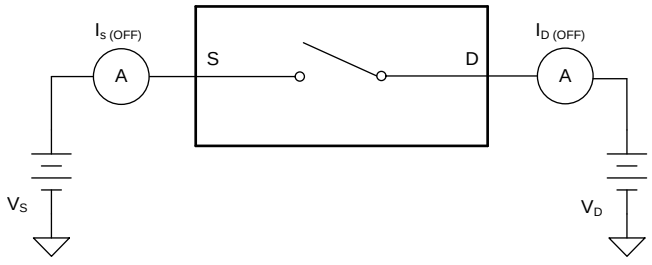


Figure 27. Off-Leakage Measurement Setup

8.4 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 28 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

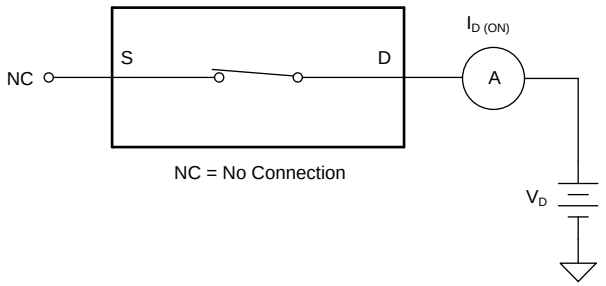


Figure 28. On-Leakage Measurement Setup

8.5 Transition Time

Transition time is defined as the time taken by the output of the MUX50x to rise or fall to 90% of the transition after the digital address signal has fallen or risen to the 50% of the transition. Figure 29 shows the setup used to measure transition time, denoted by the symbol t_t.

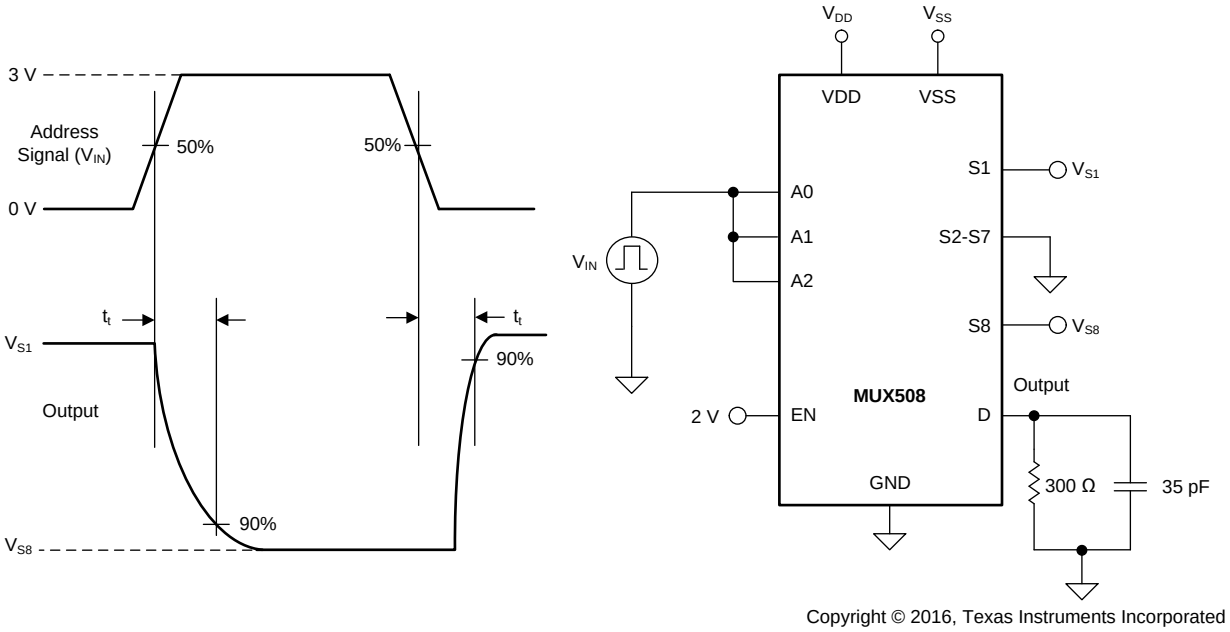


Figure 29. Transition-Time Measurement Setup

8.6 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the MUX50x is switching. The MUX50x output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as a break-before-make delay. Figure 30 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

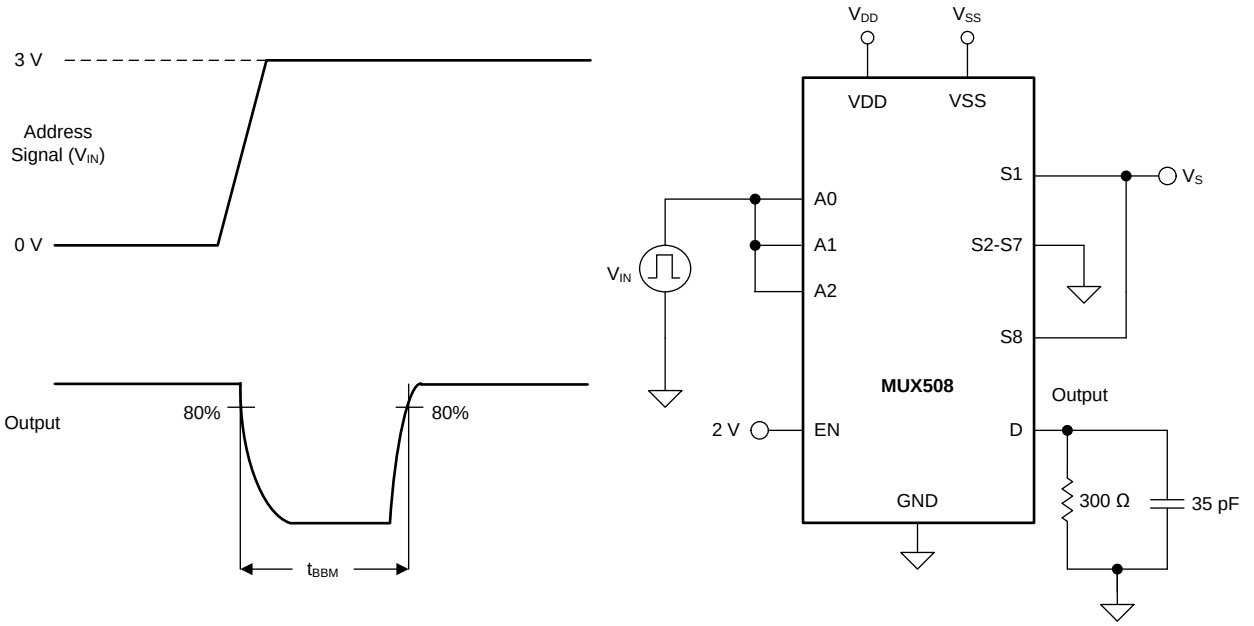


Figure 30. Break-Before-Make Delay Measurement Setup

8.7 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the MUX50x to rise to a 90% final value after the enable signal has risen to a 50% final value. Figure 31 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the MUX50x to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. Figure 31 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

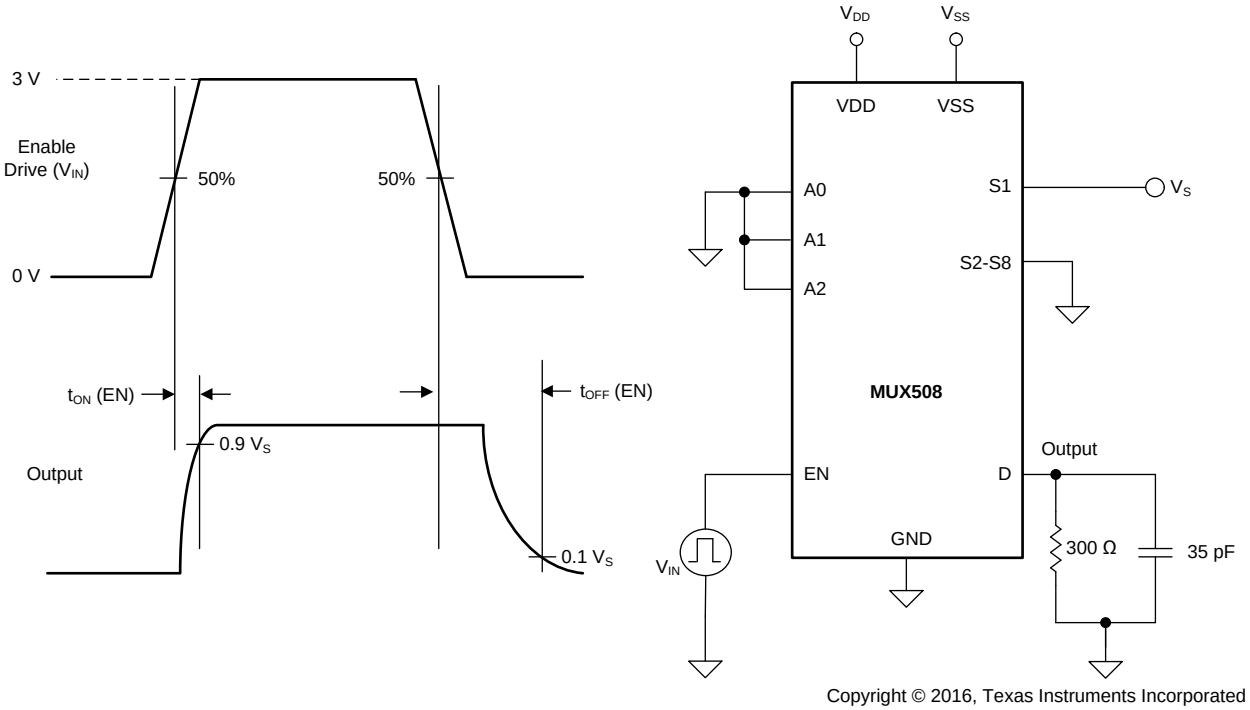


Figure 31. Turn-On and Turn-Off Time Measurement Setup

8.8 Charge Injection

The MUX50x have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 32 shows the setup used to measure charge injection.

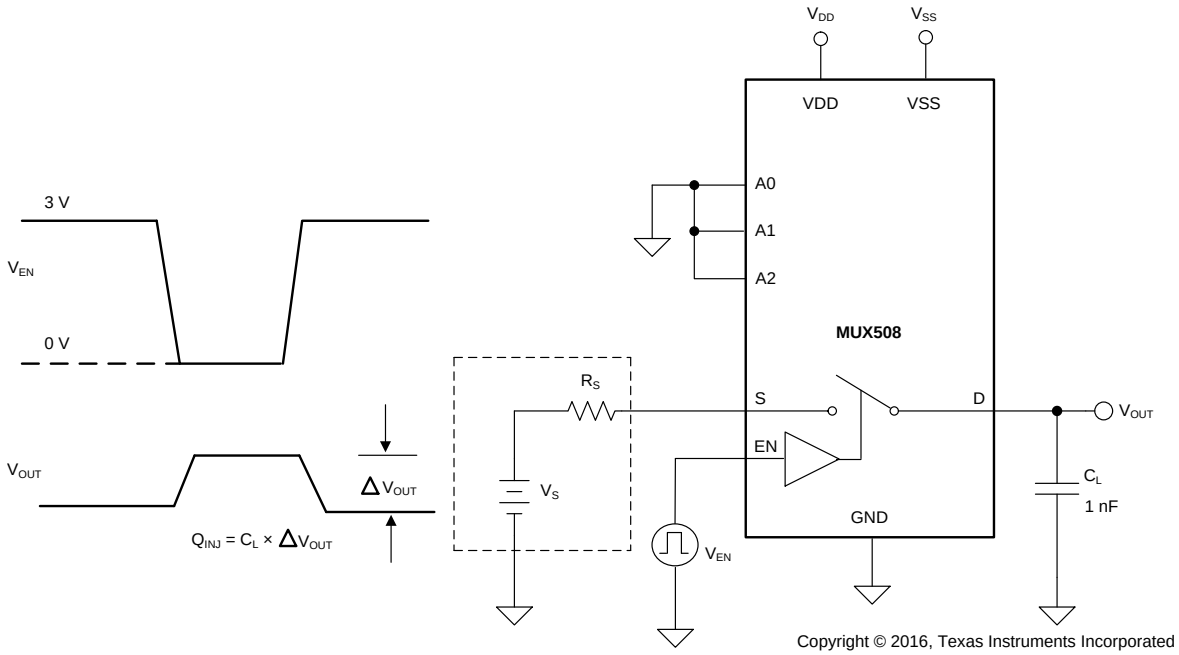


Figure 32. Charge-Injection Measurement Setup

8.9 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the MUX50x when a 1-V_{RMS} signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. Figure 33 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

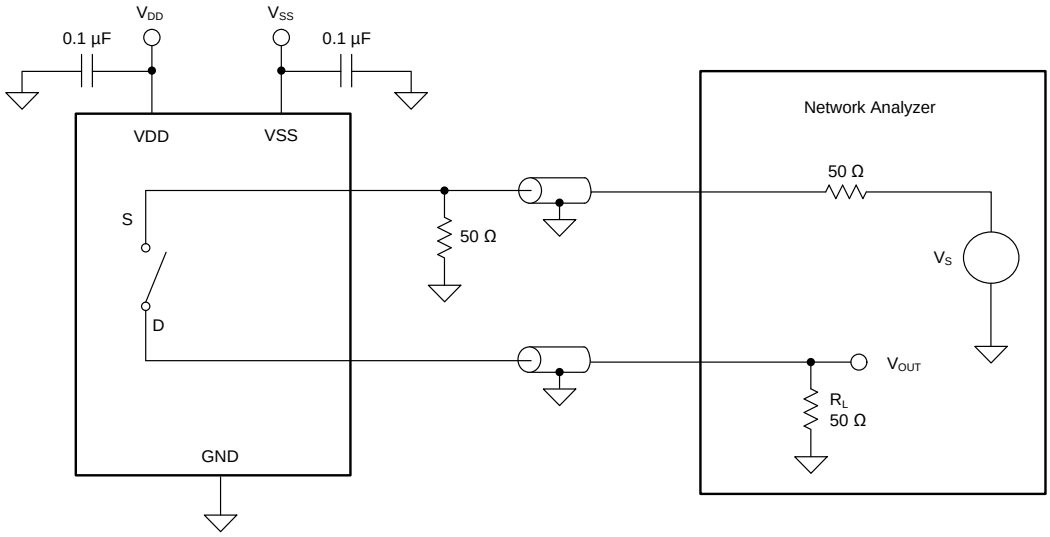


Figure 33. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

8.10 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. Figure 34 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.

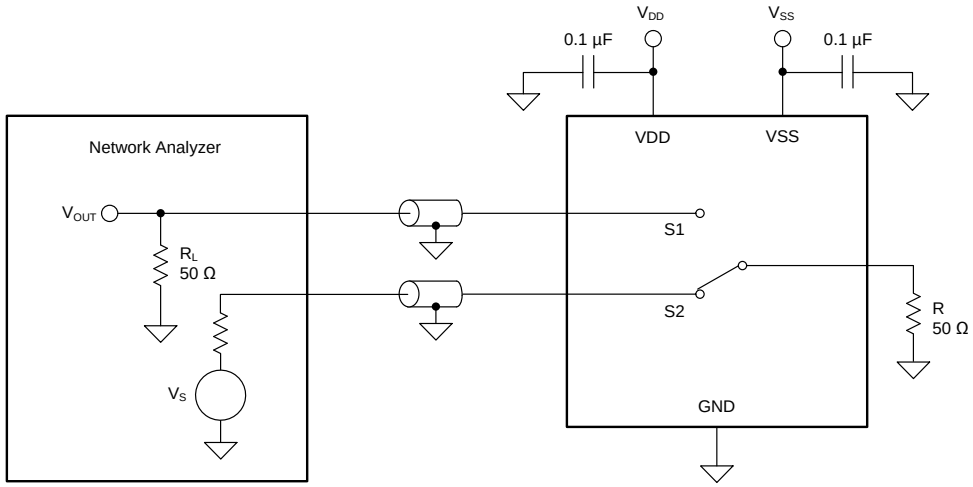


Figure 34. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

8.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin of an on-channel and the output is measured at the drain pin of the MUX50x. Figure 35 shows the setup used to measure bandwidth of the mux. Use Equation 4 to compute the attenuation.

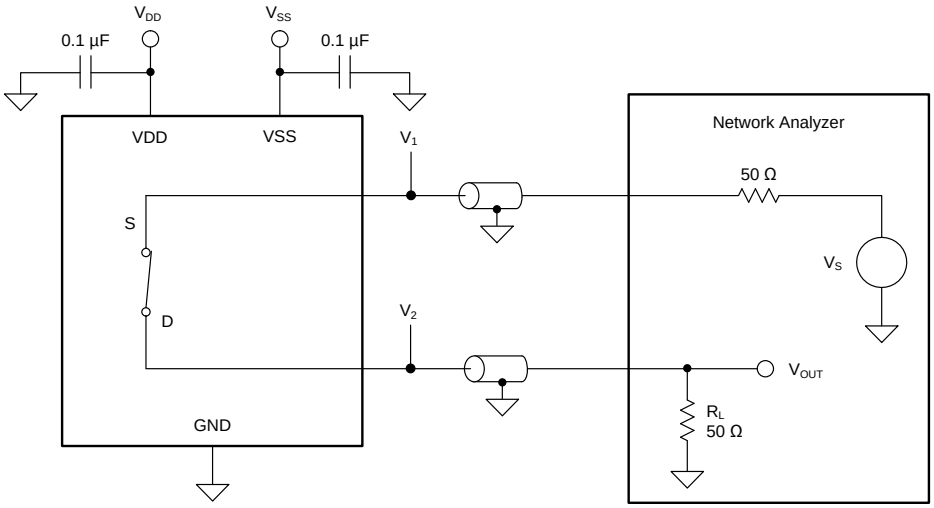


Figure 35. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{4}$$

8.12 THD + Noise

The total harmonic distortion (THD) of a signal is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the MUX50x varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 36 shows the setup used to measure the THD+N of the MUX50x.

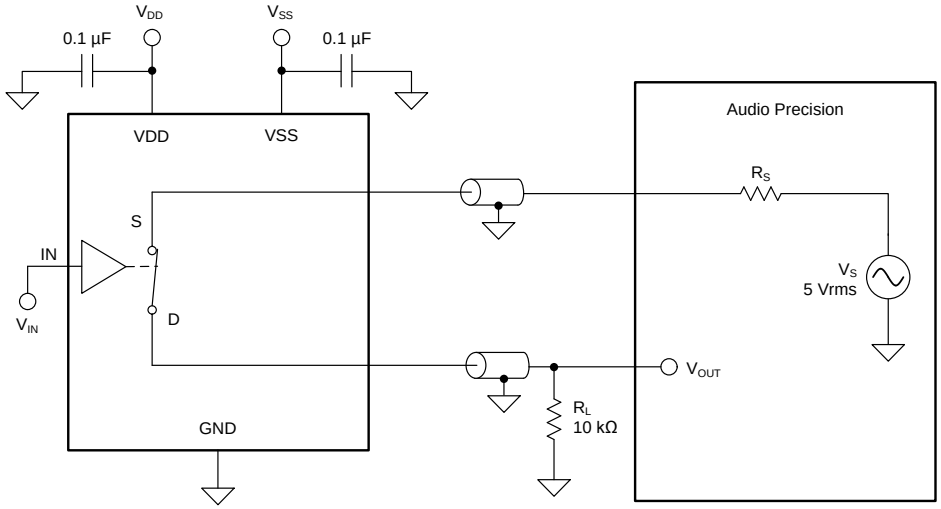


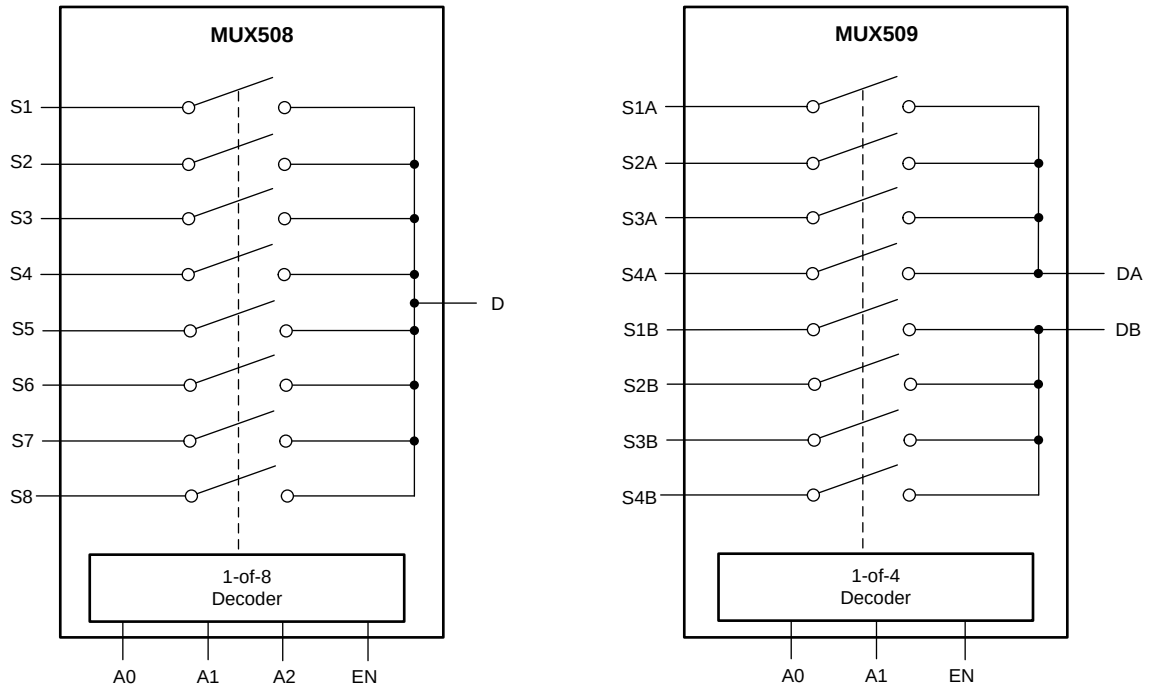
Figure 36. THD+N Measurement Setup

9 Detailed Description

9.1 Overview

The MUX50x are a family of analog multiplexers. The *Functional Block Diagram* section provides a top-level block diagram of both the MUX508 and MUX509. The MUX508 is an eight-channel, single-ended, analog mux. The MUX509 is a four-channel, differential or dual 4:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Ultralow Leakage Current

The MUX50x provide extremely low on- and off-leakage currents. The MUX50x are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of these ultralow leakage currents. Figure 37 shows typical leakage currents of the MUX50x versus temperature.

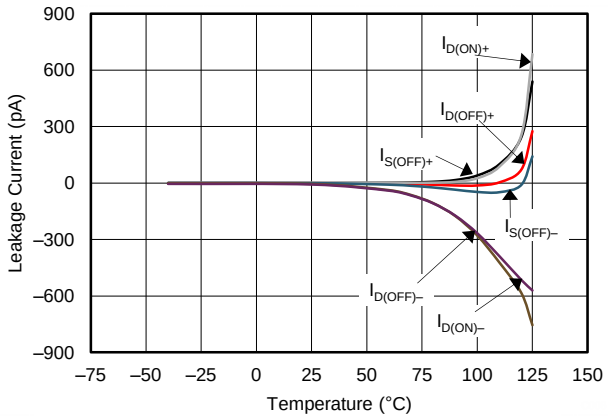


Figure 37. Leakage Current vs Temperature

9.3.2 Ultralow Charge Injection

The MUX50x have a simple transmission gate topology, as shown in Figure 38. Any mismatch in the stray capacitance associated with the NMOS and PMOS transistors creates an output level change whenever the switch is opened or closed.

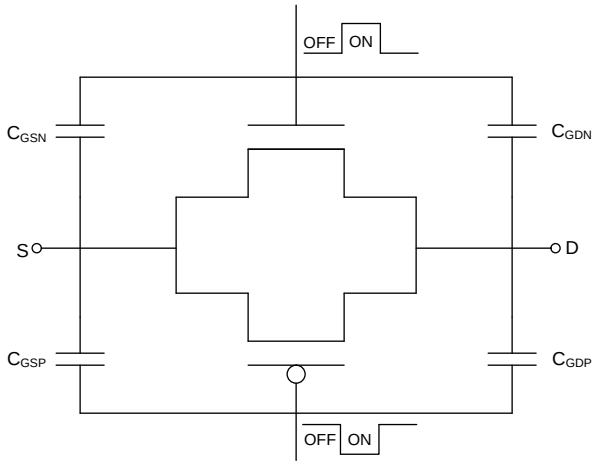


Figure 38. Transmission Gate Topology

Feature Description (continued)

The MUX50x have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 0.3 pC at V_S = 0 V, and ±0.6 pC in the full signal range, as shown in Figure 39.

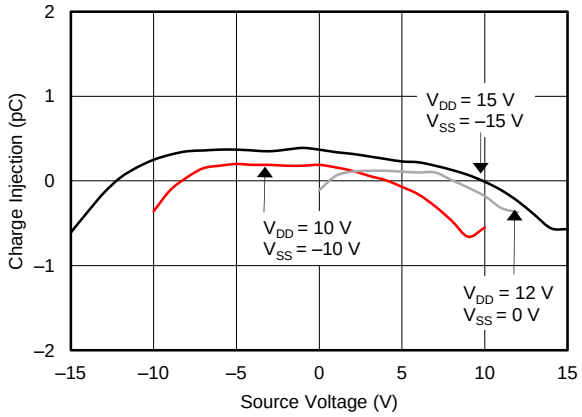


Figure 39. Source-to-Drain Charge Injection vs Source or Drain voltage

The drain-to-source charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. Figure 40 shows the drain-to-source charge injection across the full signal range.

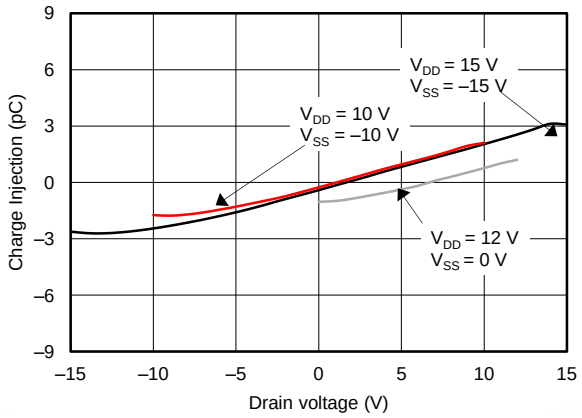


Figure 40. Drain-to-Source Charge Injection vs Source or Drain voltage

9.3.3 Bidirectional Operation

The MUX50x are operable as both a mux or demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the MUX50x are used either as input or output. Each MUX50x channel has very similar characteristics in both directions.

Feature Description (continued)

9.3.4 Rail-to-Rail Operation

A valid analog signal for the MUX50x ranges from V_{SS} to V_{DD}. The input signal to the MUX50x can swing from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of the MUX50x varies with input signal, as shown in Figure 41.

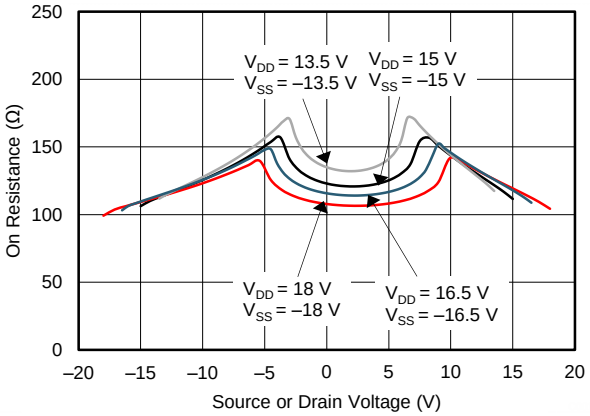


Figure 41. On-Resistance vs Source or Drain Voltage

9.4 Device Functional Modes

When the EN pin of the MUX50x is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 36 V).

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The MUX50x family offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the MUX50x is very low. These features makes the MUX50x a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

10.2 Typical Application

Figure 42 shows a 16-bit, differential, four-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a four-channel differential mux. This application example details the process for optimizing a precision, high-voltage, front-end drive circuit using the MUX509, OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

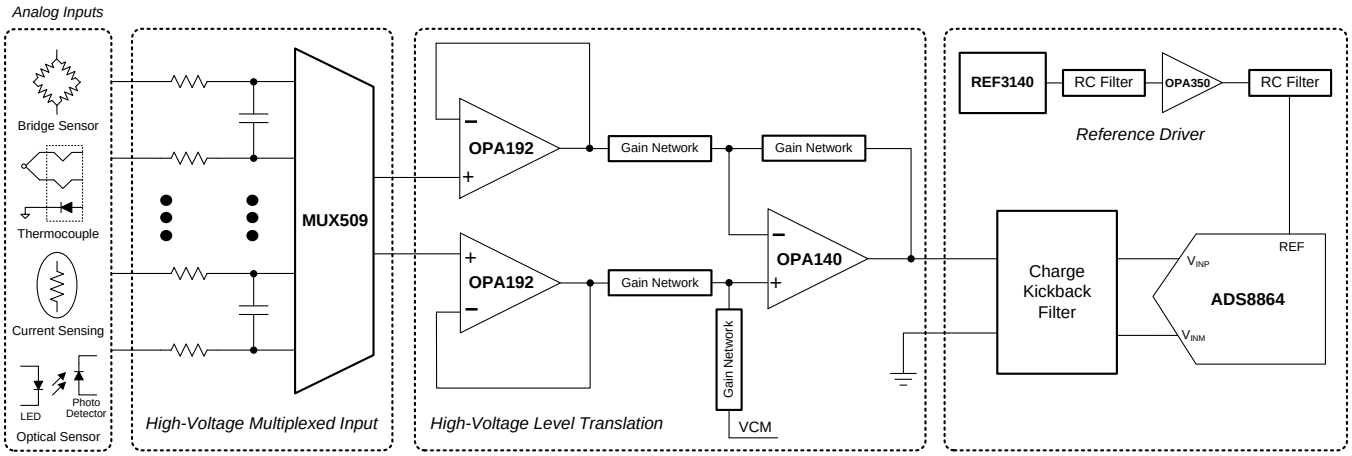


Figure 42. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

10.2.1 Design Requirements

The primary objective is to design a ±20 V, differential, four-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ±15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 20 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

Typical Application (continued)

10.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in Figure 42. The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel.

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see TI Precision Design TIPD151, *16-Bit, 400-kSPS, 4-Channel Multiplexed Data-Acquisition System for High-Voltage Inputs with Lowest Distortion*.

10.2.3 Application Curve

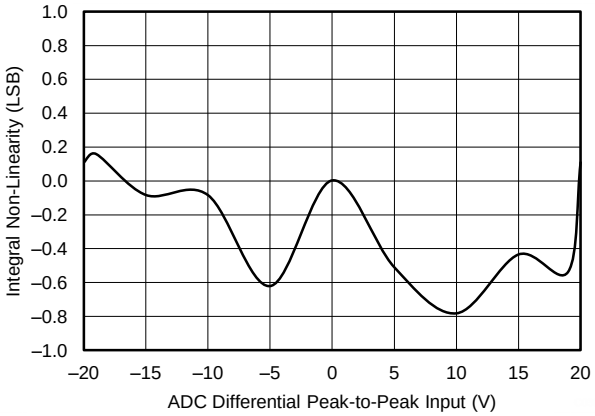


Figure 43. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

11 Power-Supply Recommendations

The MUX50x operates across a wide supply range of ±5 V to ±18 V (10 V to 36 V in single-supply mode). The MUX508 and MUX509 operate equally well with either dual supplies (±5 V to ±18 V), or a single supply (10 V to 36 V). They also perform well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS} = –5 V. For reliable operation, use a supply decoupling capacitor with a capacitance between 0.1 µF to 10 µF at both the VDD and VSS pins to ground.

The on-resistance of the MUX50x varies with supply voltage, as shown in Figure 44.

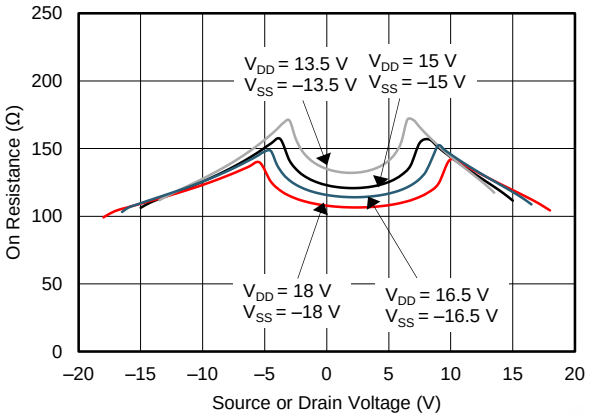


Figure 44. On-Resistance Variation With Supply and Input Voltage

12 Layout

12.1 Layout Guidelines

Figure 45 shows an example of a PCB layout with the MUX508IPW, and Figure 46 shows an example of a PCB layout with MUX509IPW. The guidelines provided in this section are also applicable to the SOIC MUX508ID and MUX509ID package variants as well.

Some key considerations are:

1. Decouple the VDD and VSS pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as small as possible. For the MUX509 differential signals, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when necessary.

12.2 Layout Example

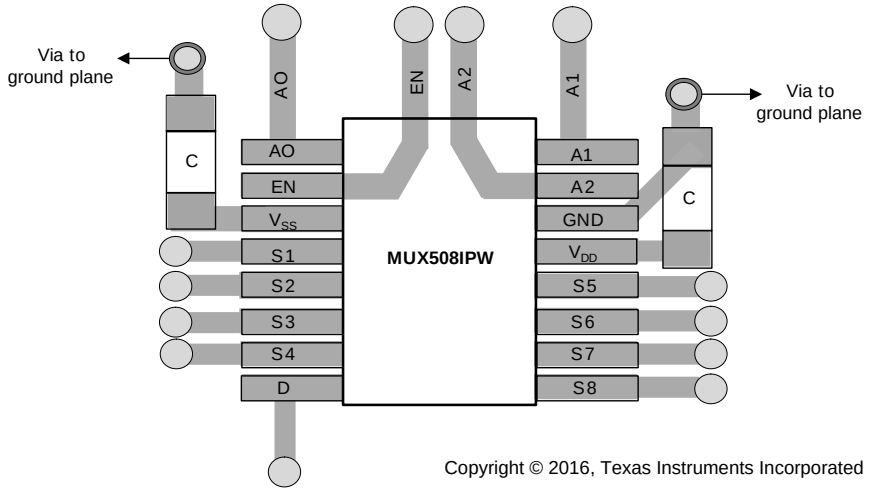


Figure 45. MUX508IPW Layout Example

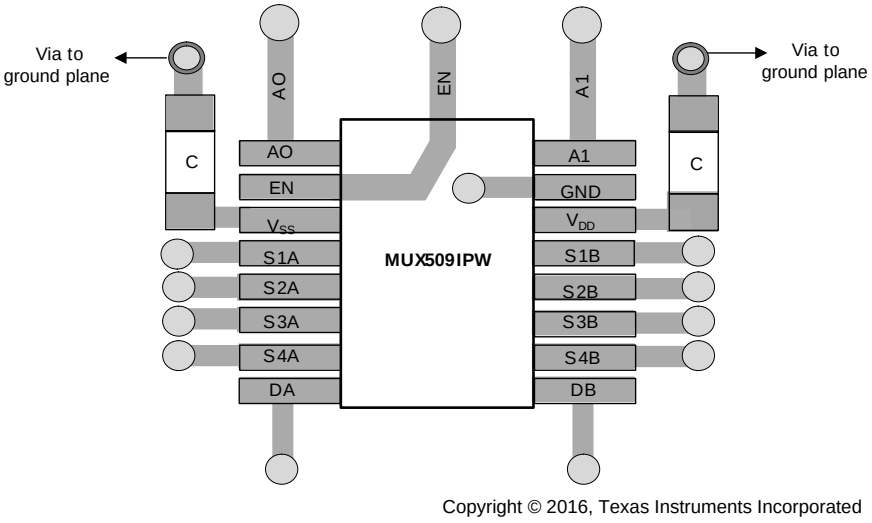


Figure 46. MUX509IPW Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

- *ADS866x 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges* (SBAS492)
- *OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz JFET Op Amp* (SBOS498)
- *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™* (SBOS620)

13.2 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MUX508	Click here	Click here	Click here	Click here	Click here
MUX509	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MUX508ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	M36508D
MUX508ID.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M36508D
MUX508IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	M36508D
MUX508IDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M36508D
MUX508IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX508IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX508IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX508IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX508IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX508IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX508B
MUX509ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	M36509D
MUX509ID.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M36509D
MUX509IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	M36509D
MUX509IDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M36509D
MUX509IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C
MUX509IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C
MUX509IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C
MUX509IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C
MUX509IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C
MUX509IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MUX509C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

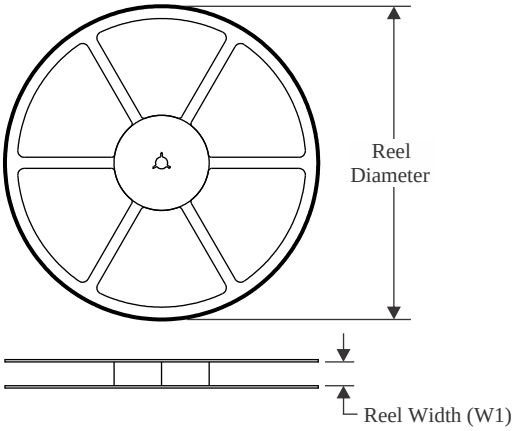
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

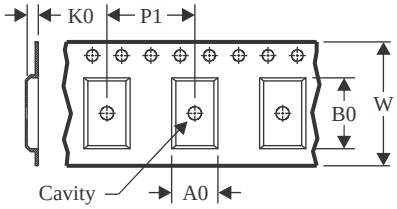
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

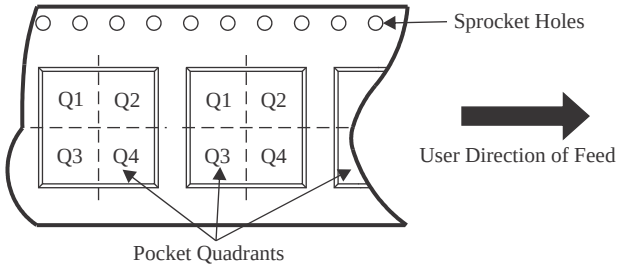


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



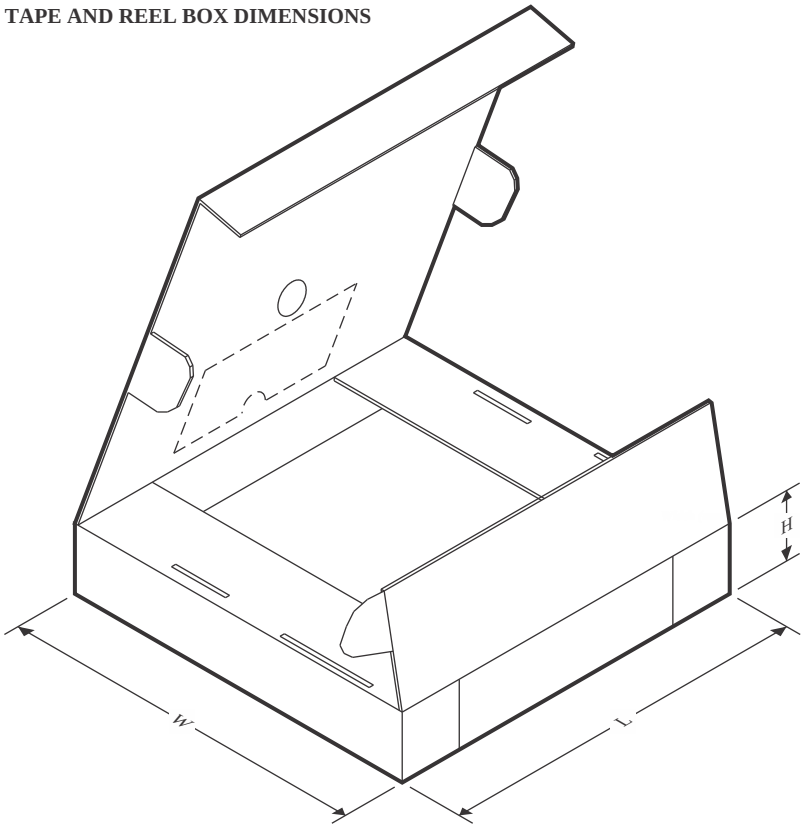
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MUX508IDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
MUX508IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX508IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX509IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MUX509IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

18-Jun-2025

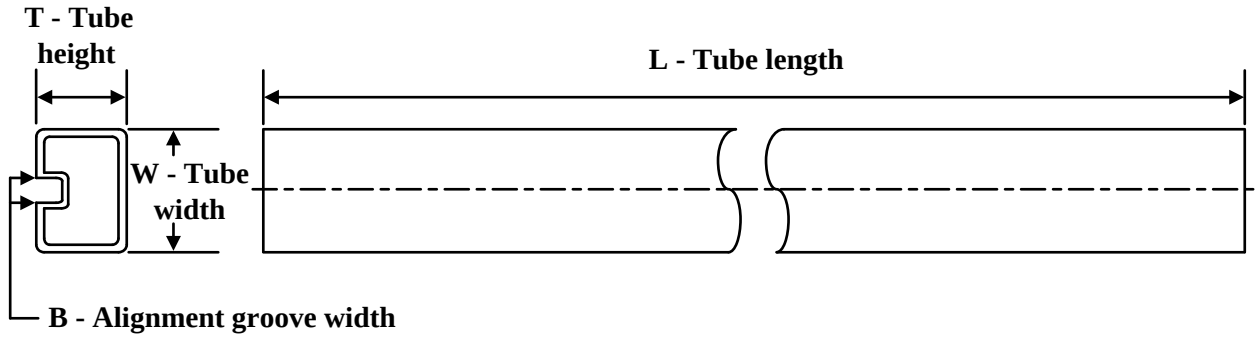
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MUX508IDR	SOIC	D	16	2500	366.0	364.0	50.0
MUX508IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MUX508IPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
MUX509IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MUX509IPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

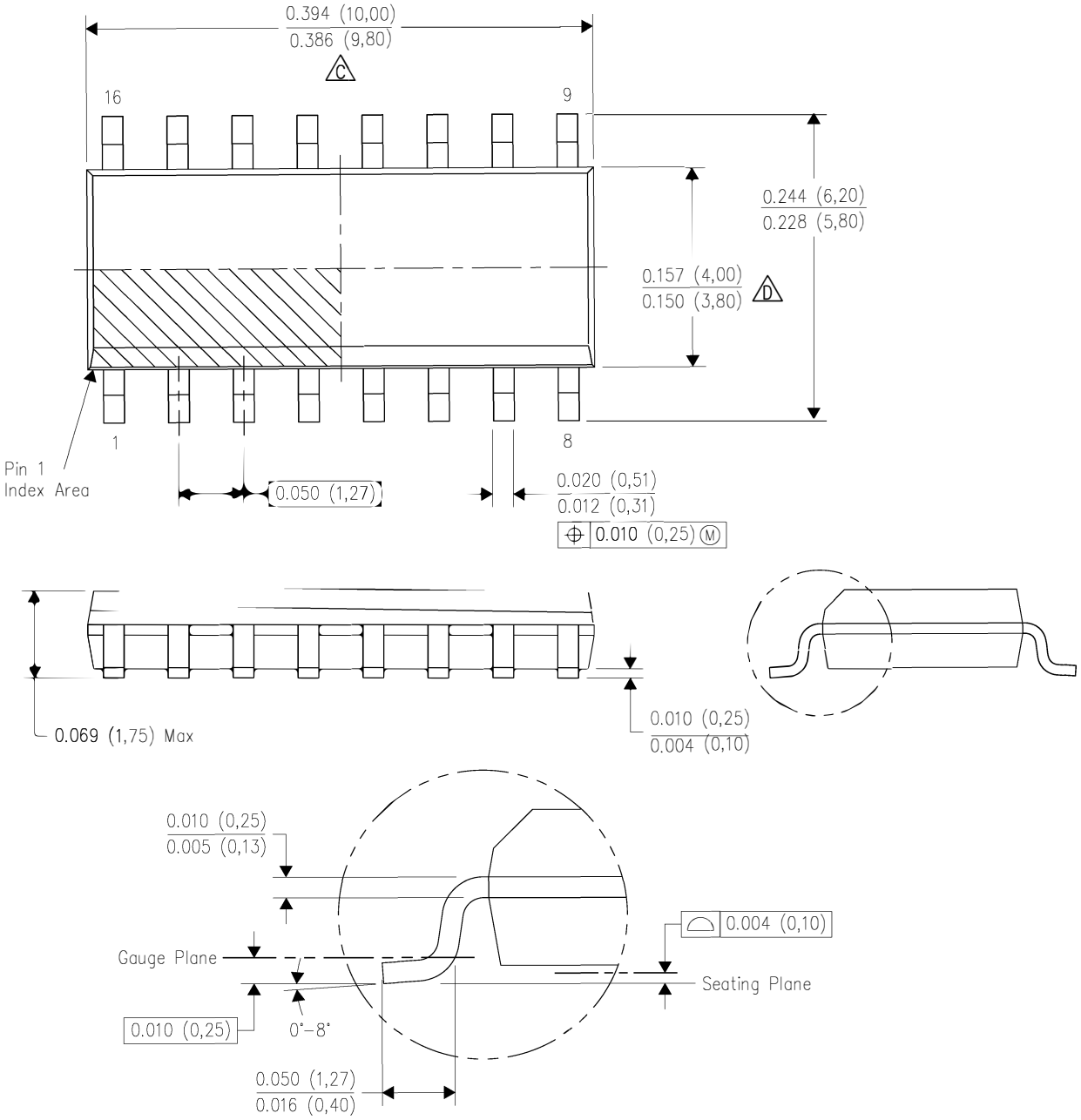
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MUX508ID	D	SOIC	16	40	507	8	3940	4.32
MUX508ID	D	SOIC	16	40	517	7.87	635	4.25
MUX508ID.B	D	SOIC	16	40	517	7.87	635	4.25
MUX508ID.B	D	SOIC	16	40	507	8	3940	4.32
MUX508IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX508IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX509ID	D	SOIC	16	40	507	8	3940	4.32
MUX509ID	D	SOIC	16	40	517	7.87	635	4.25
MUX509ID.B	D	SOIC	16	40	507	8	3940	4.32
MUX509ID.B	D	SOIC	16	40	517	7.87	635	4.25
MUX509IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MUX509IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



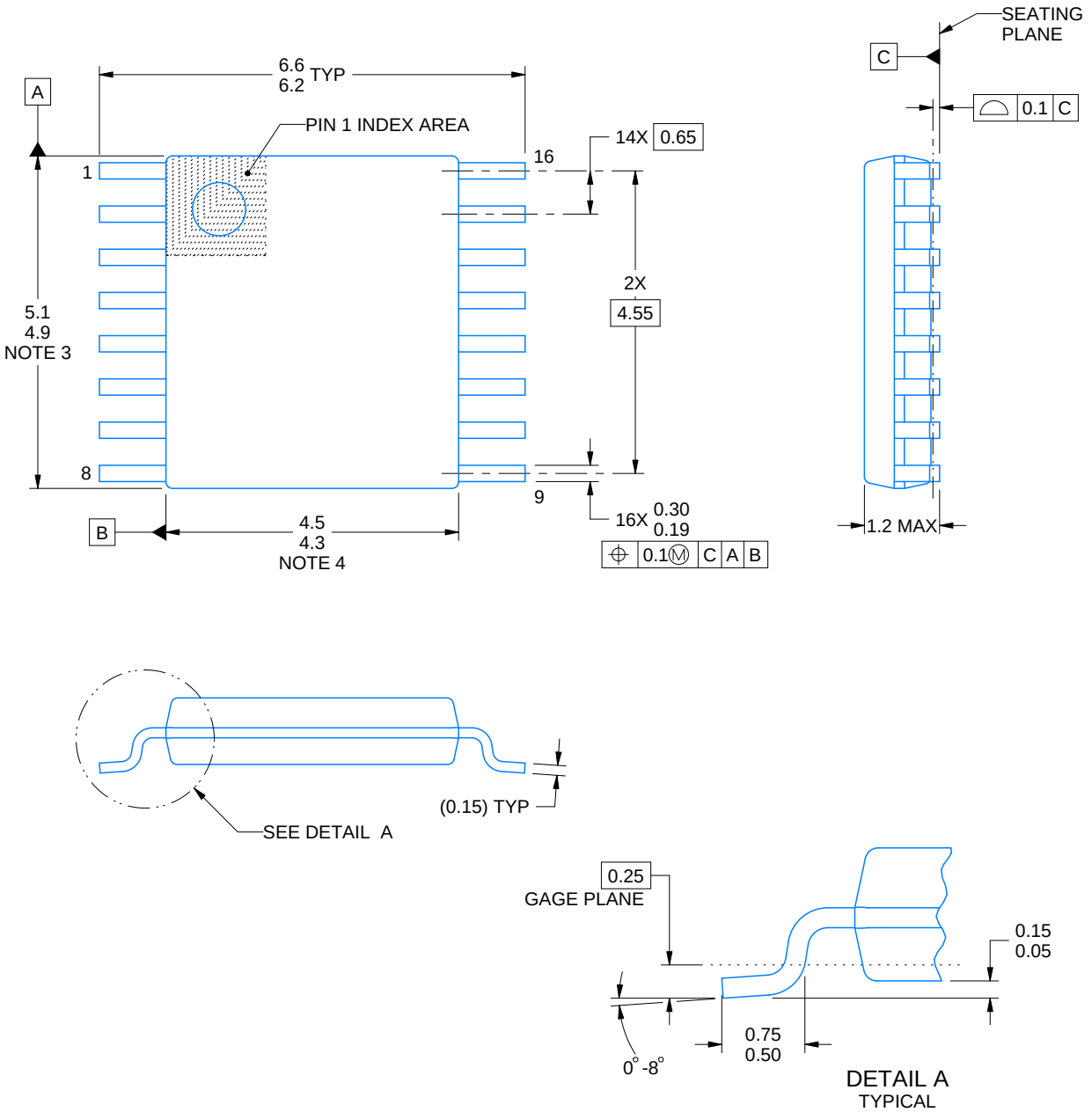
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

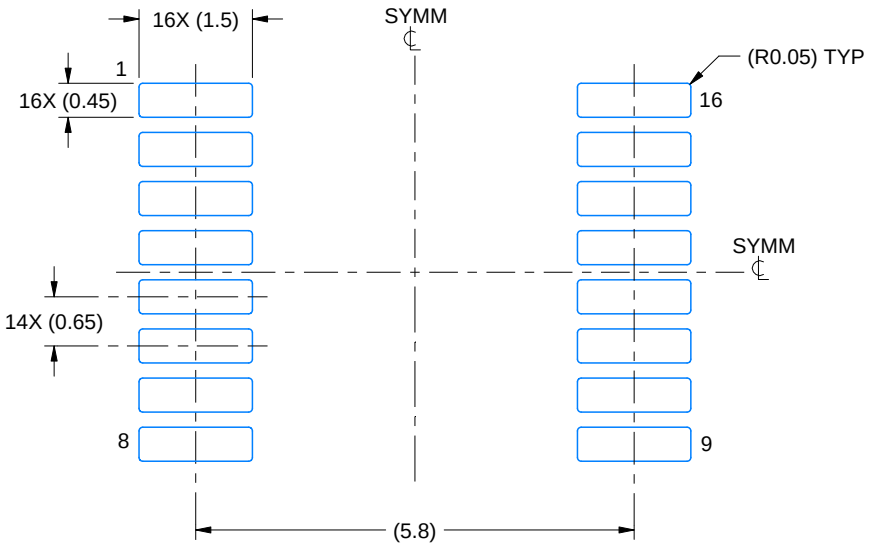
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

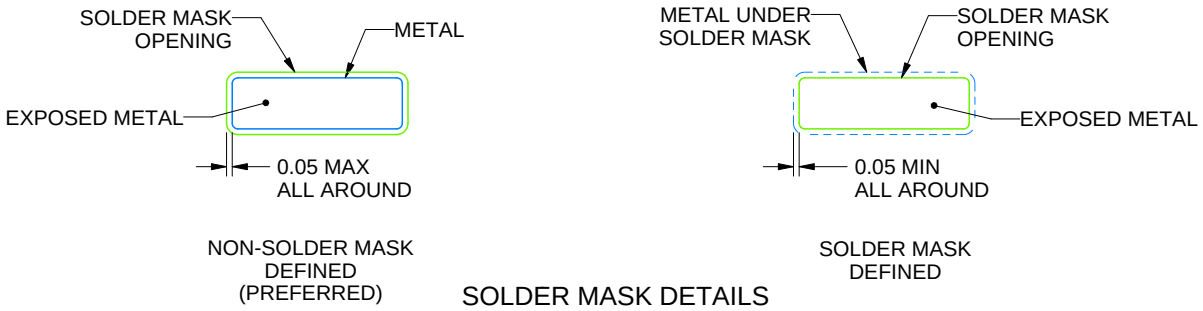


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

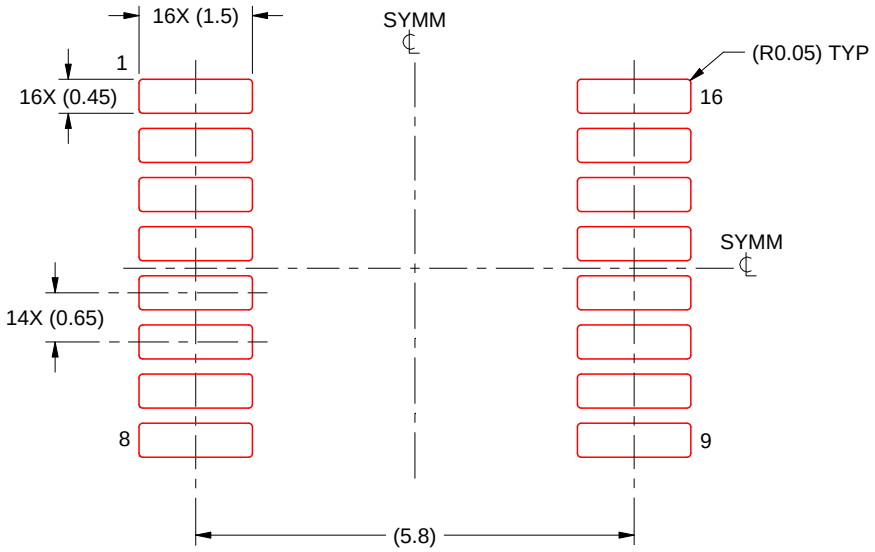
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.